

Internet Anwendungen unter z/OS und OS/390

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WS 2004/2005

Teil 1 b

zSeries Hardware

Lochschriftübersetzung

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1 2 4 6 8 10	12 14 16 18 20 22 24 26 28 30 32 34	36 38 40 42 44 46	48 50 52 54 56 58 60 62 64 66 68 70 72 74 76 78 80					

Überlochzone

Normallochzone

Zeile

Lochfeld der Ziffern 0-9

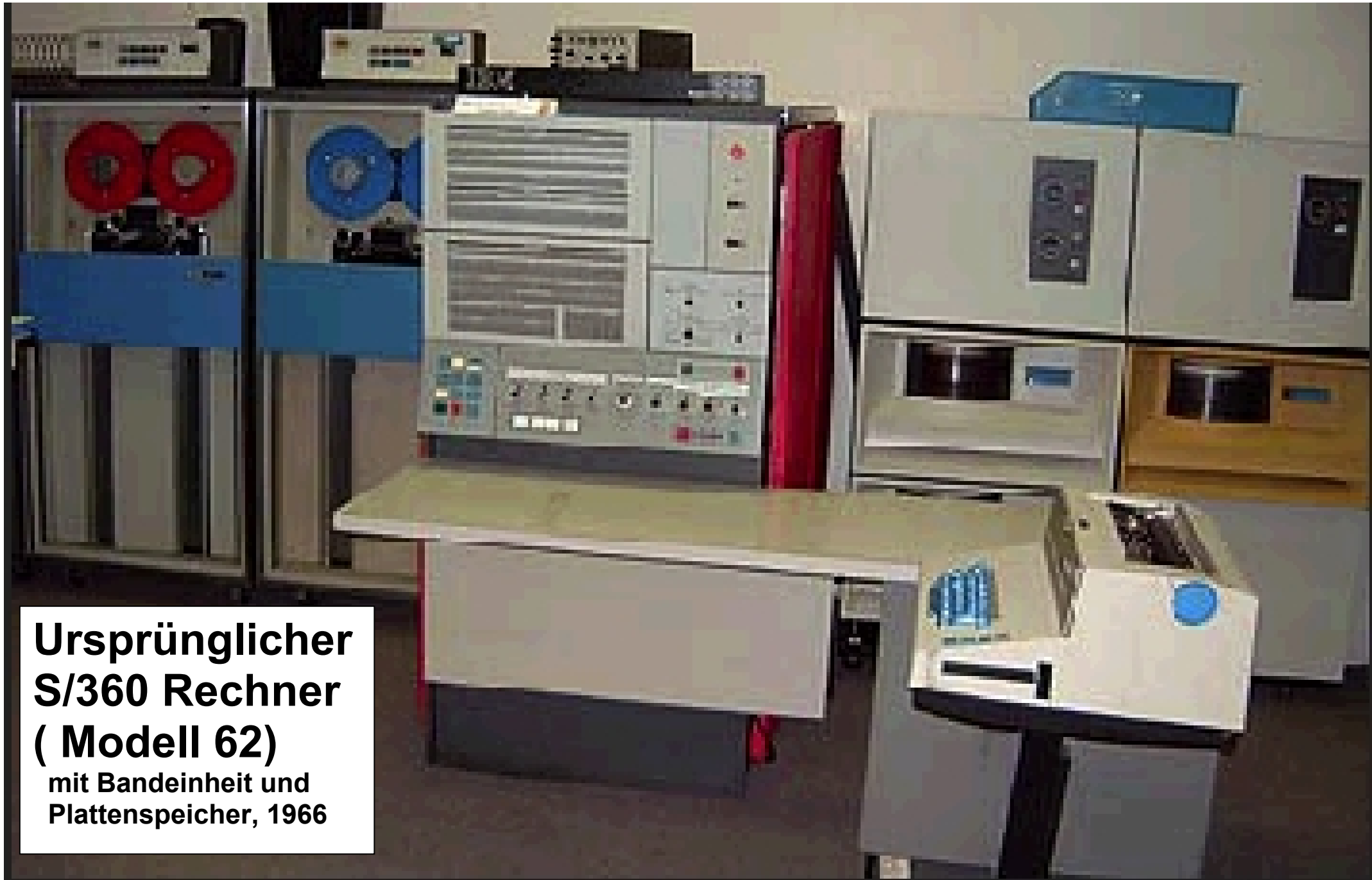
Spalte

Lochposition

IBM Lochkarte

IBM 026 Card Punch

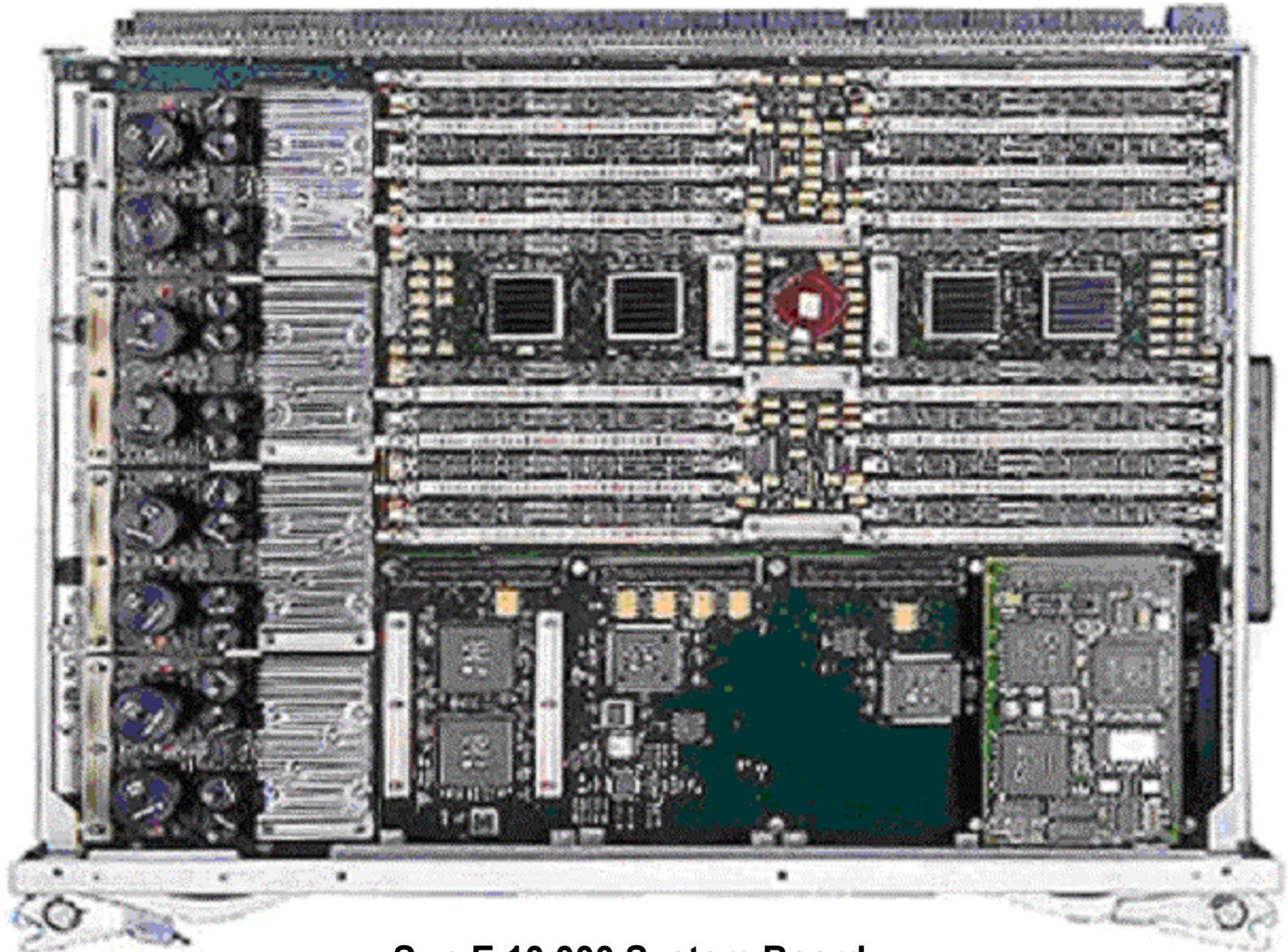




**Ursprünglicher
S/360 Rechner
(Modell 62)
mit Bandeinheit und
Plattenspeicher, 1966**

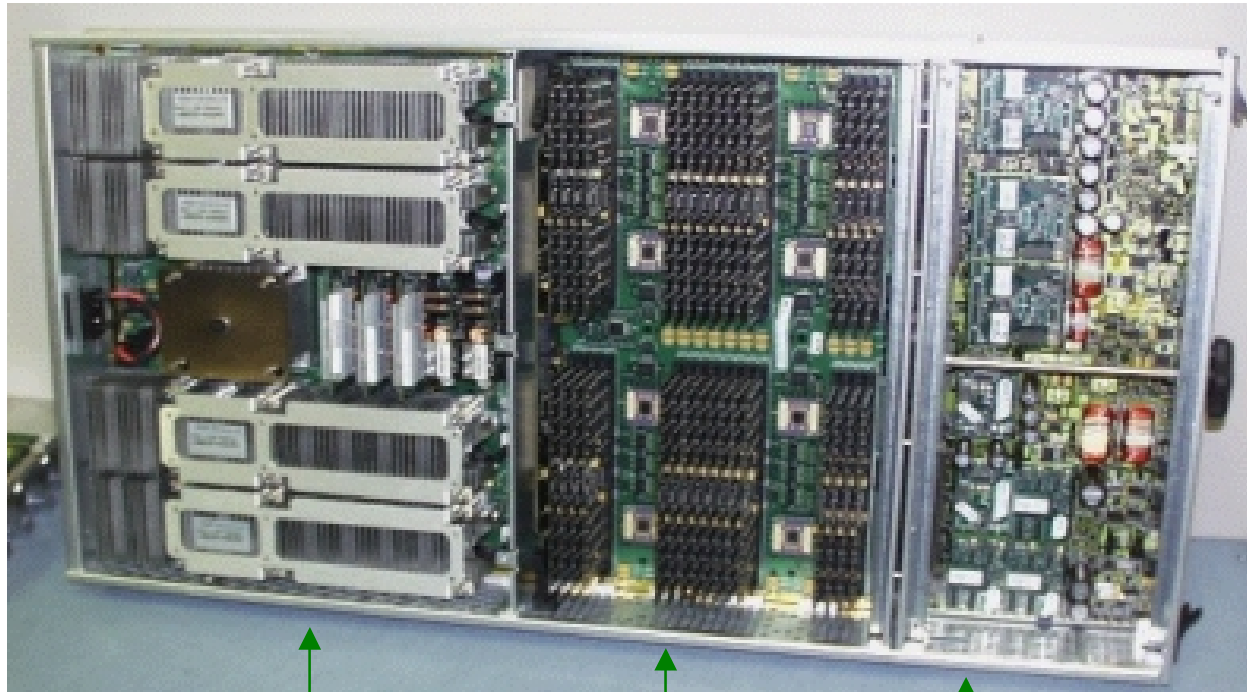


IBM 3278 „Green Screen“ Bildschirm



Sun E 10 000 System Board

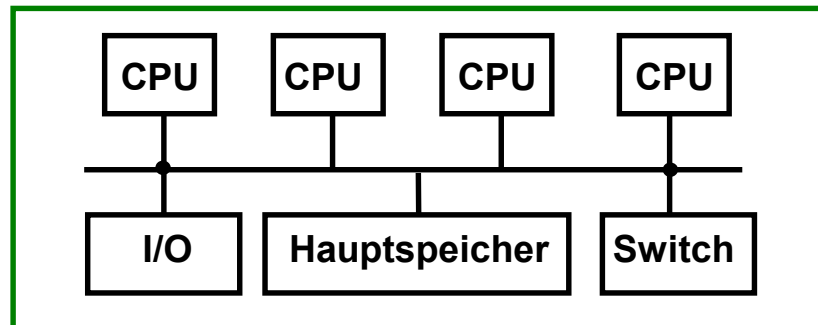
HP Superdome Cell Board

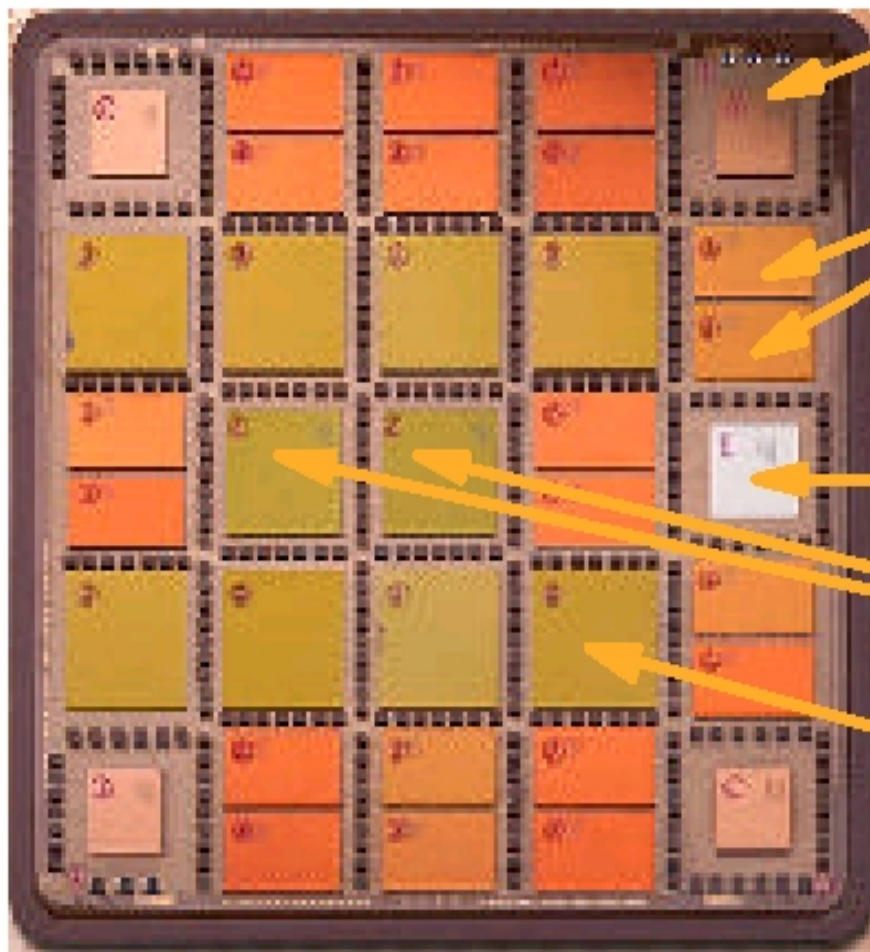


4 Itanium 2 CPUs
1,5 GHz

32 Gbyte
Hauptspeicher

E/A Bus
Anschlüsse
12 PCI





(4) Memory Bus Adapters

(20) Dual Processors:
CPU, System Assist,
Internal Coupling,
Integrated Linux, Spares

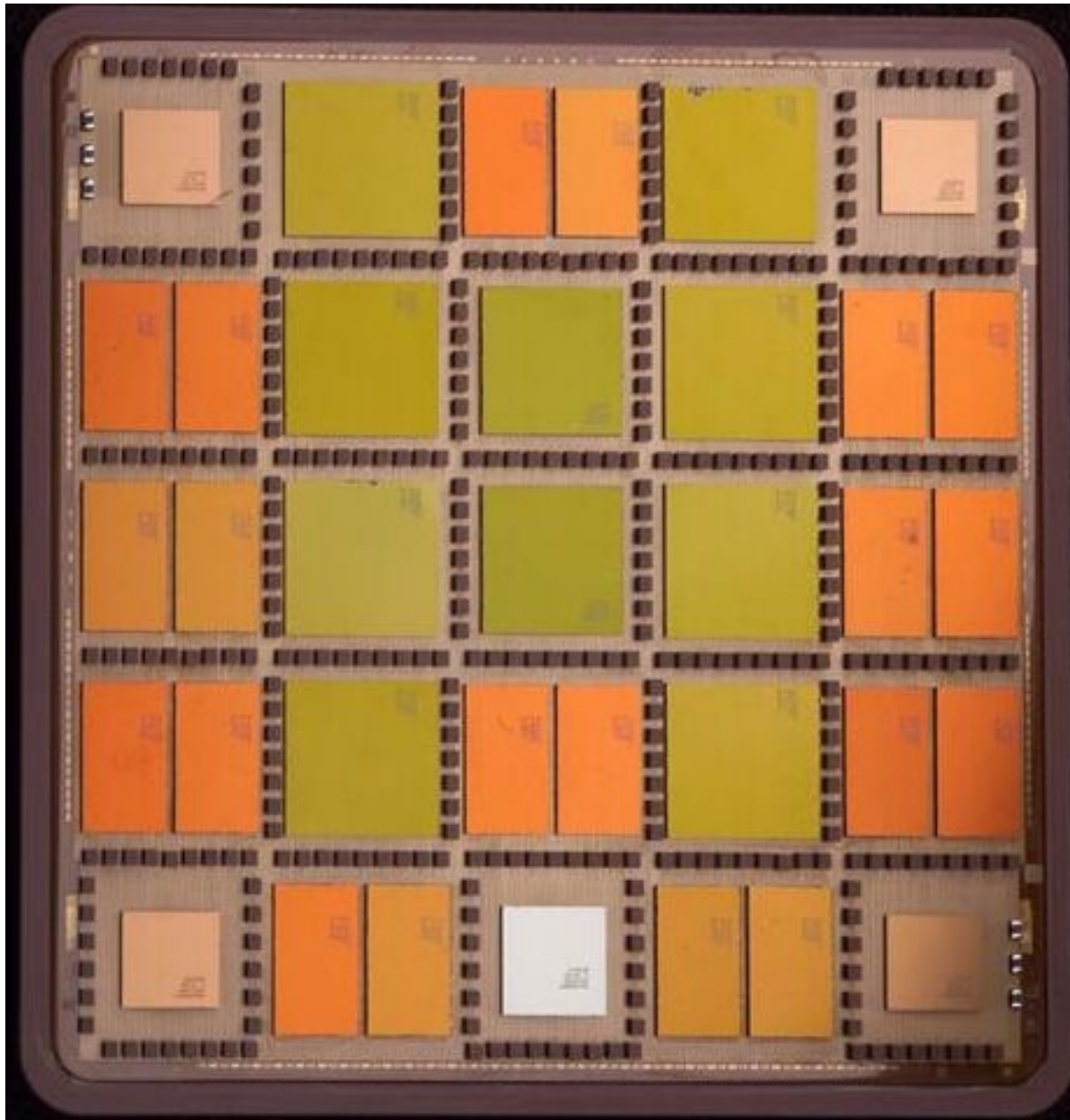
(1) Clock Chip

(2) L2 Storage Control

(8) CMOS L2 Chips

z900 Multi Chip Modul

16 CPU Chip SMP, Shared L2 Cache mit Error Correction (ECC),



Z900 Multichip Module (MCM)

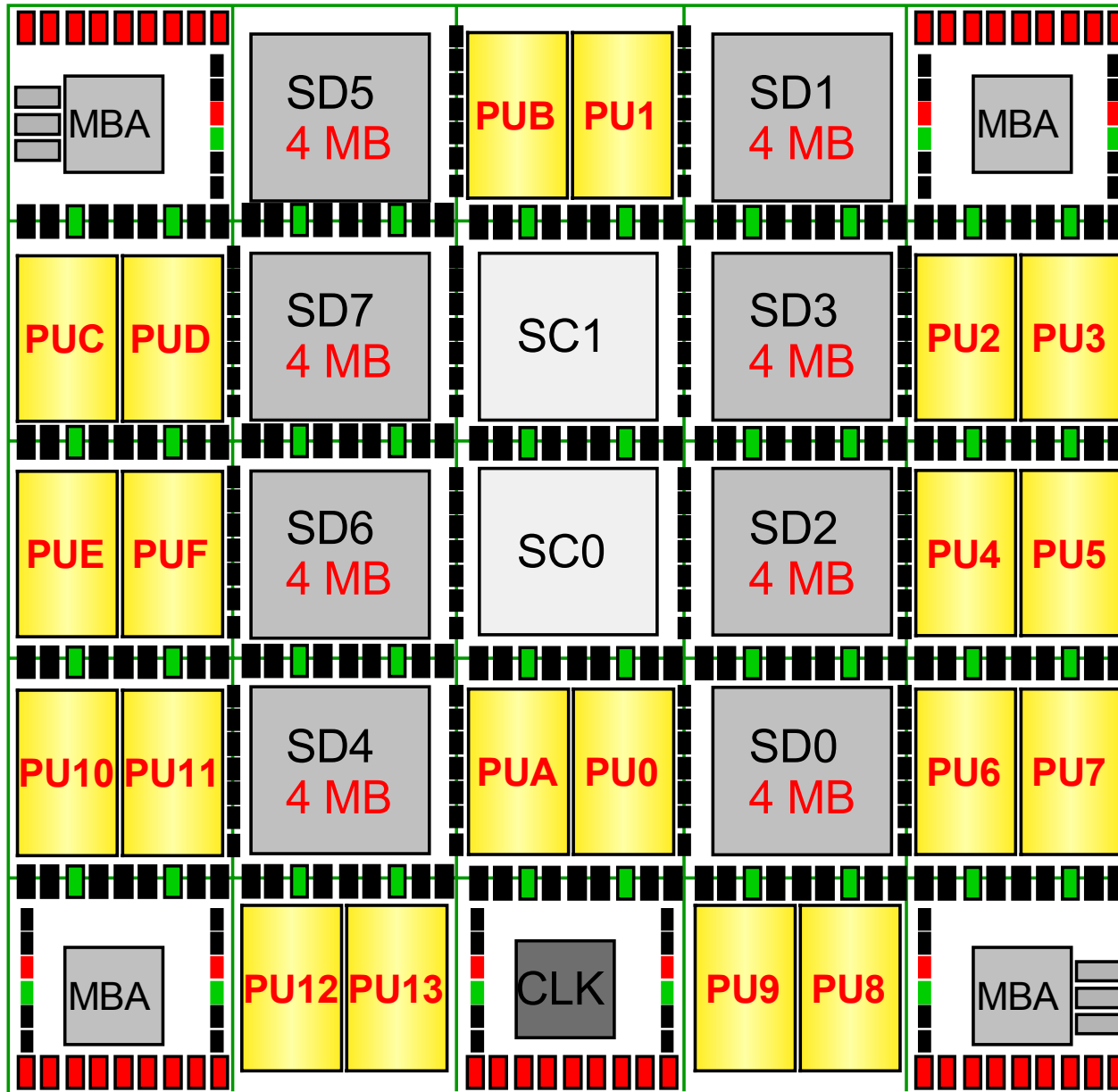
127,5 x 127,5 mm Modul

**35 Chips, 2,5 Milliarden
Transistoren**

234 Million Transistoren L2 chip

**101 Glas-Keramik + 6 Dünnschicht
Verdrahtungslagen**

1 km Drahtlänge insgesamt



Z900 Multichip Module (MCM)

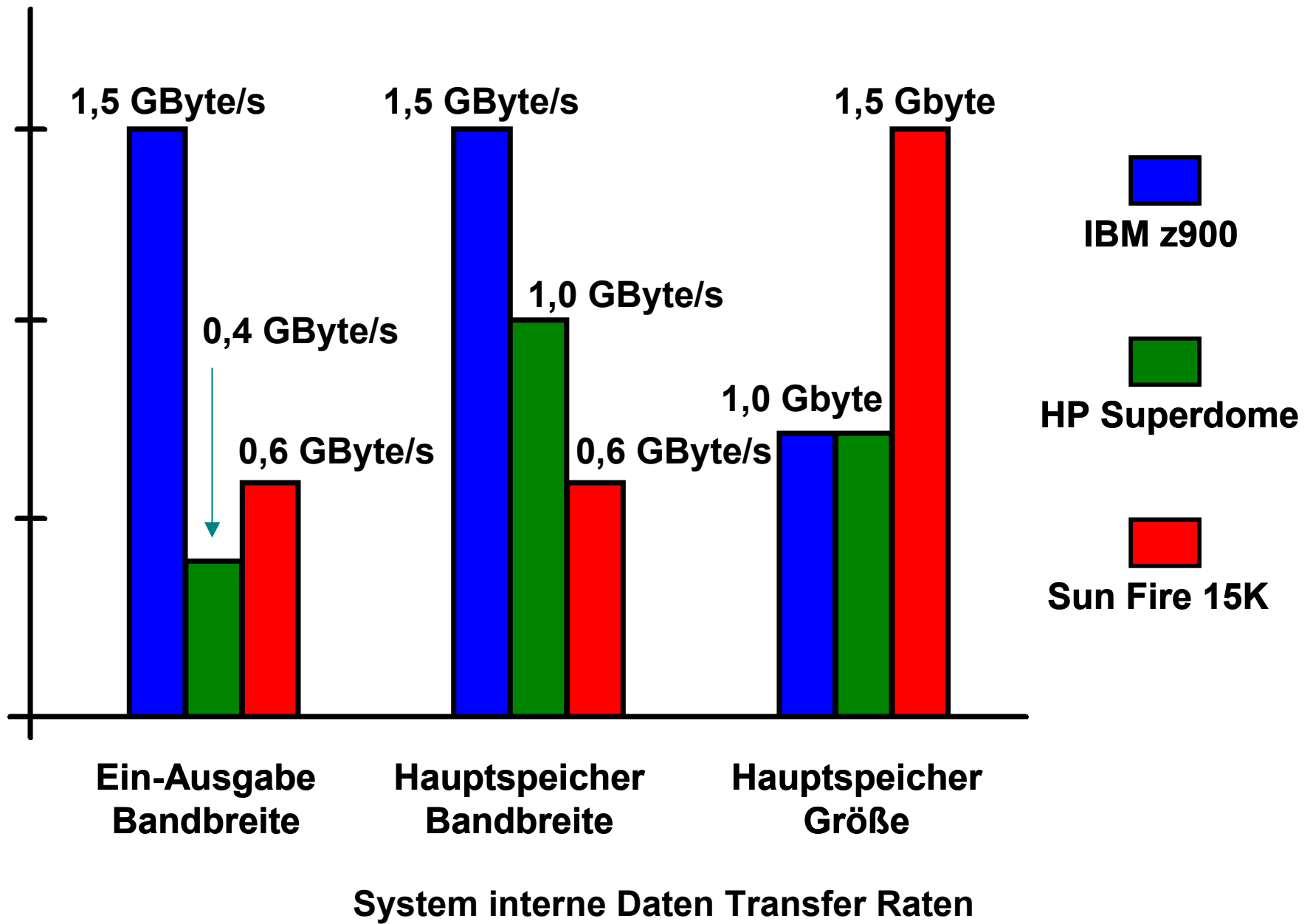
20 Mikroprozessor Chips,
16 CPU, 3 Channel Subsystem,
1 Spare

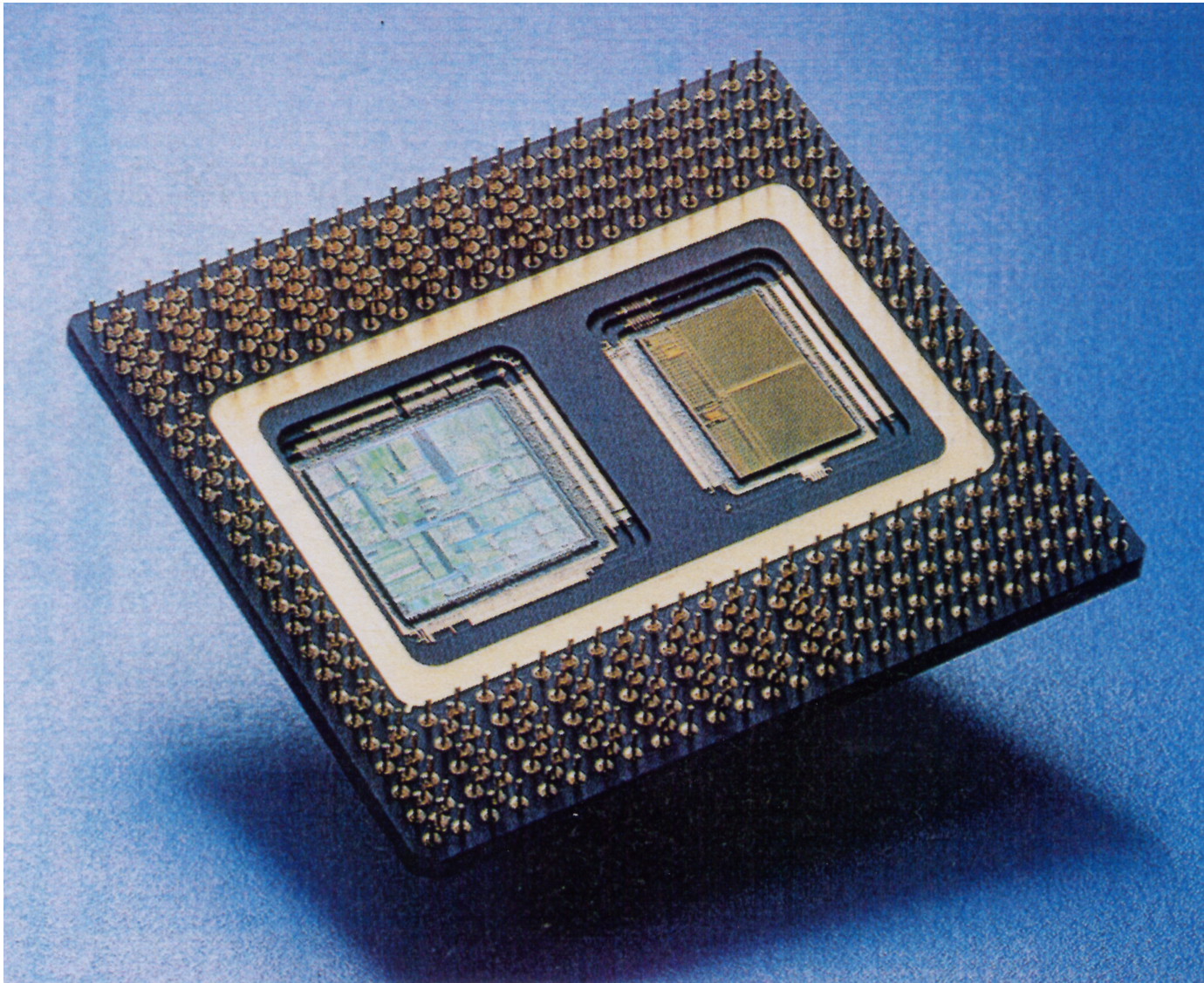
8 L2 Cache Chips, je 4 Mbyte,
je 234 Mill. Transistoren

2 Storage Control Chips

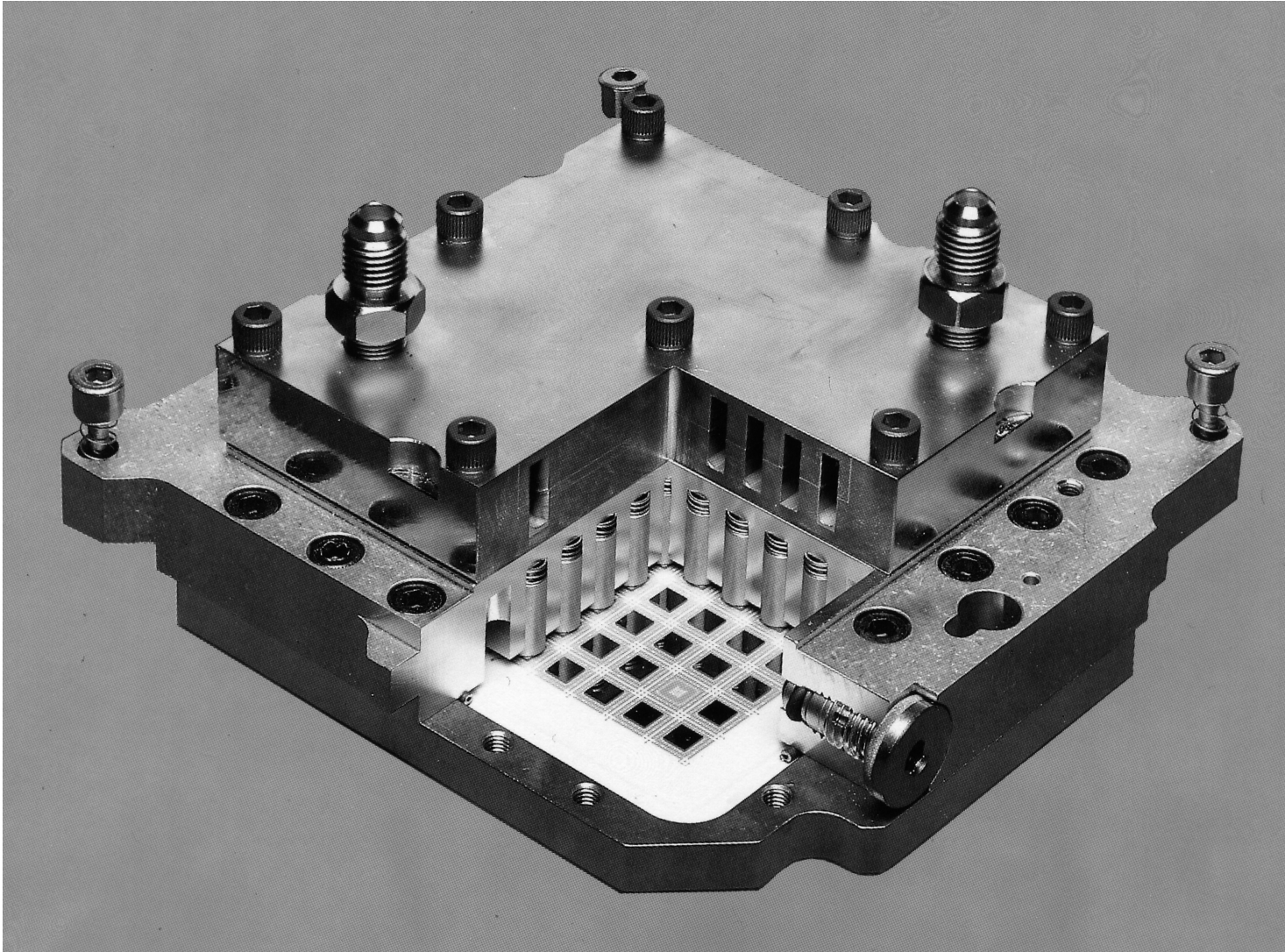
4 Memory Bus Adapter Chips

1 Clock Chip

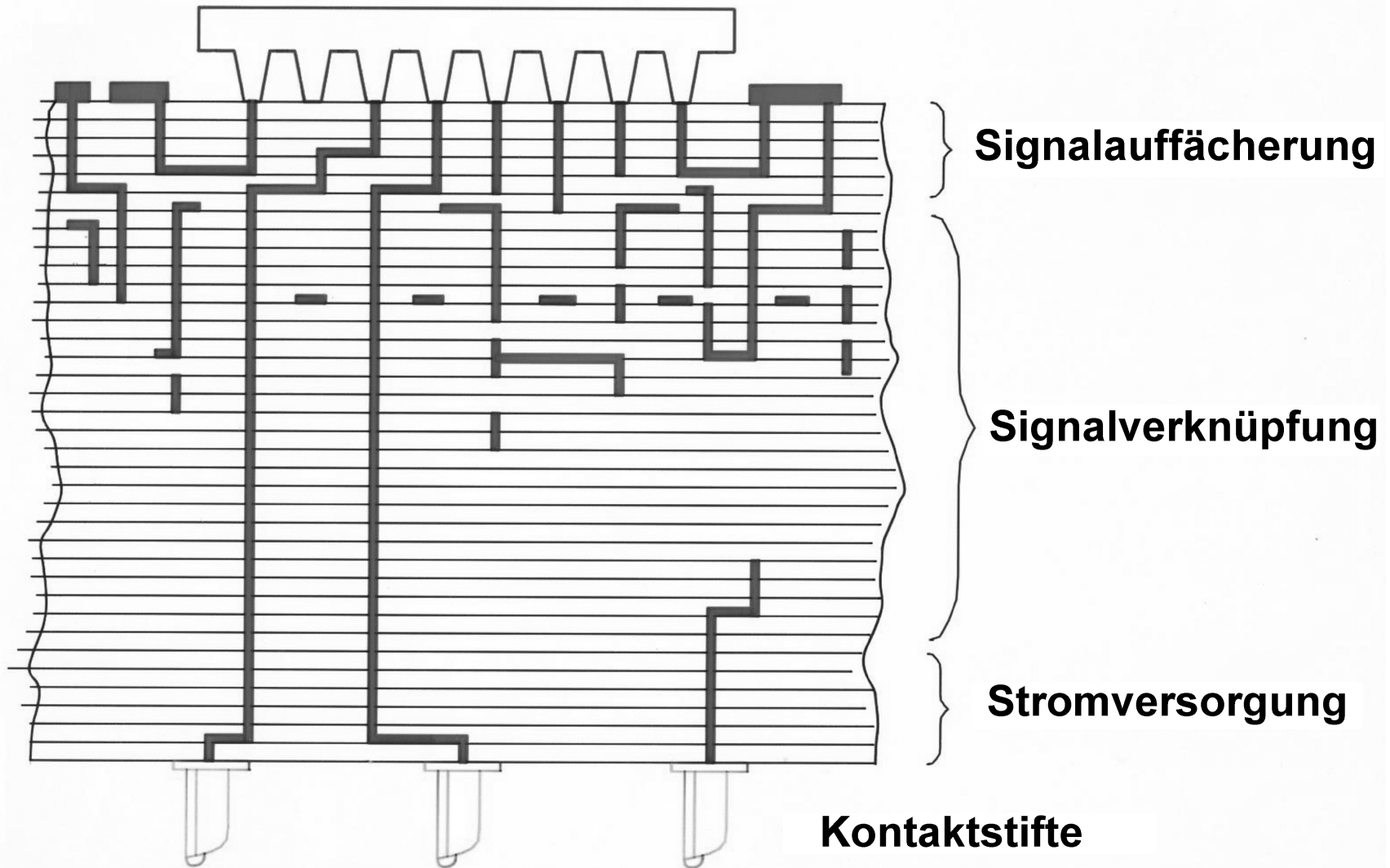




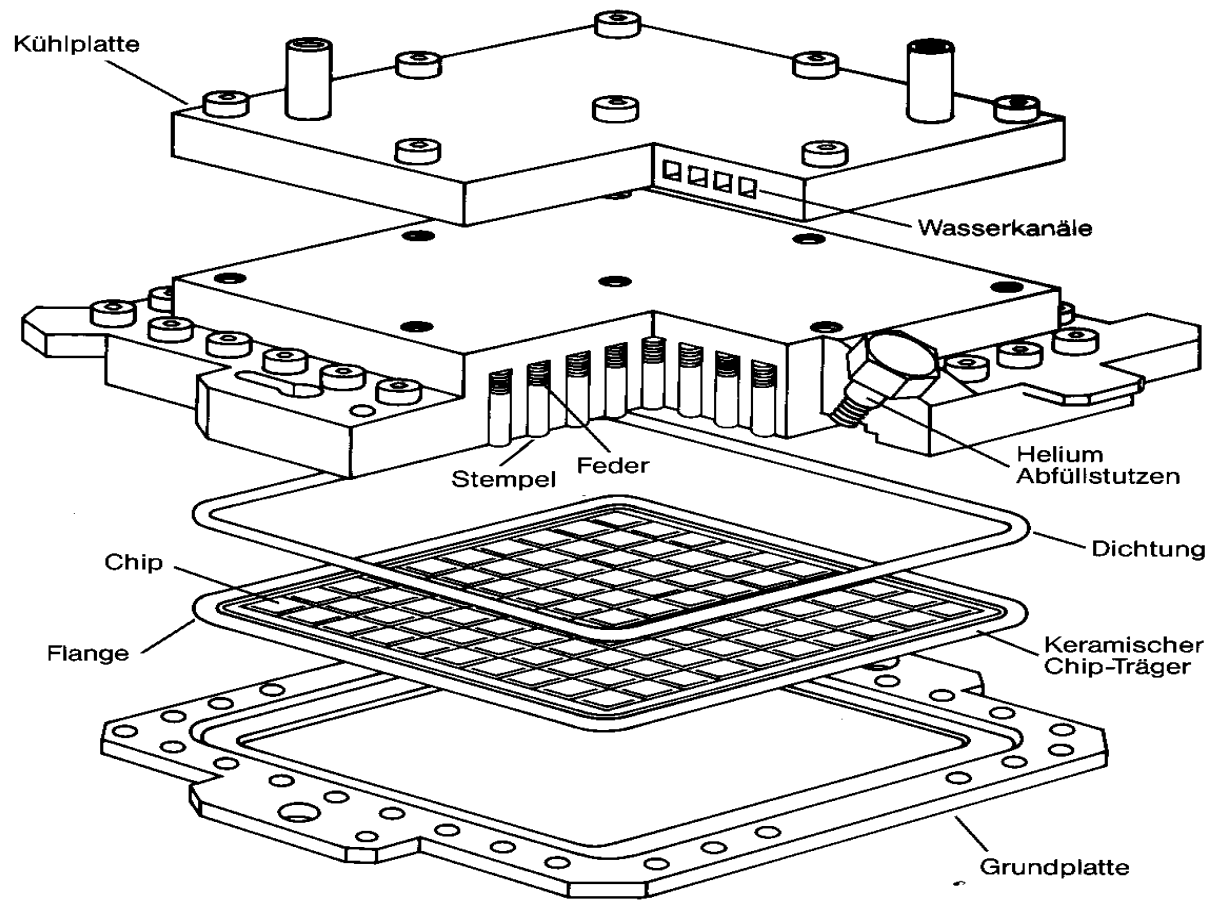
Pentium Pro
387 Pin Multi Layer Ceramic (MLC) Multi Chip Carrier (MCM) Module



Thermal Conduction Module (TCM)

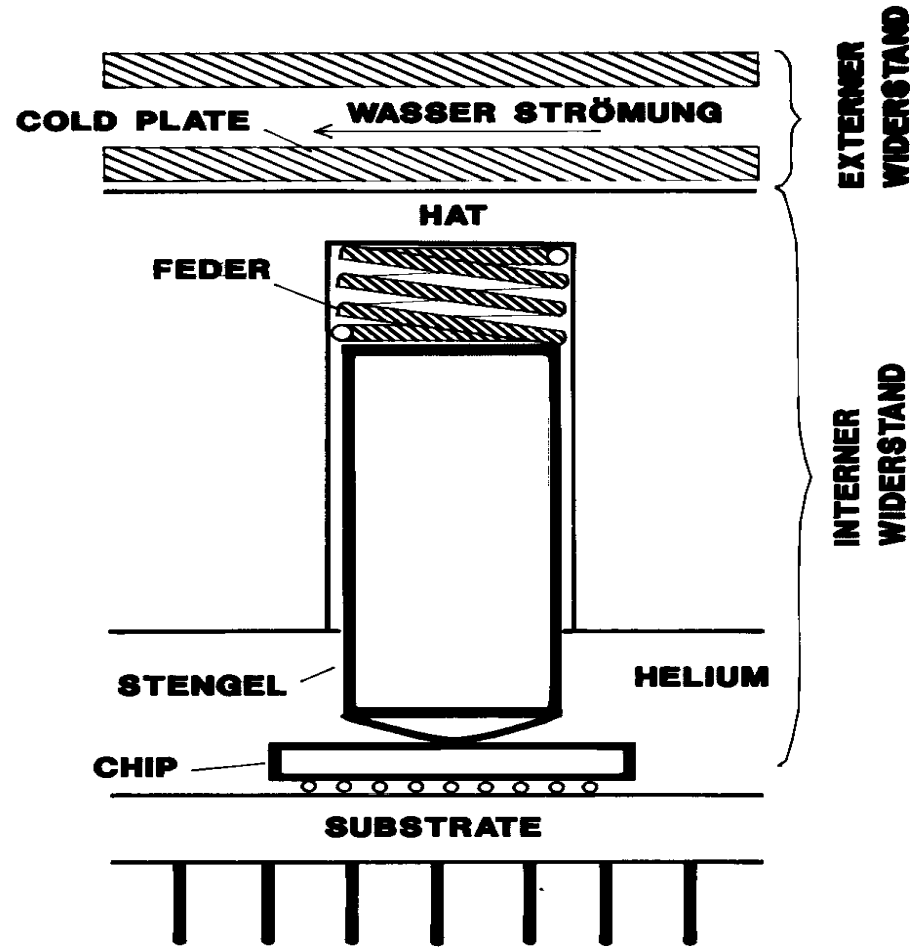


101 + 6 Schichten, über 4000 Kontaktstifte
1 km Verdrahtungslänge



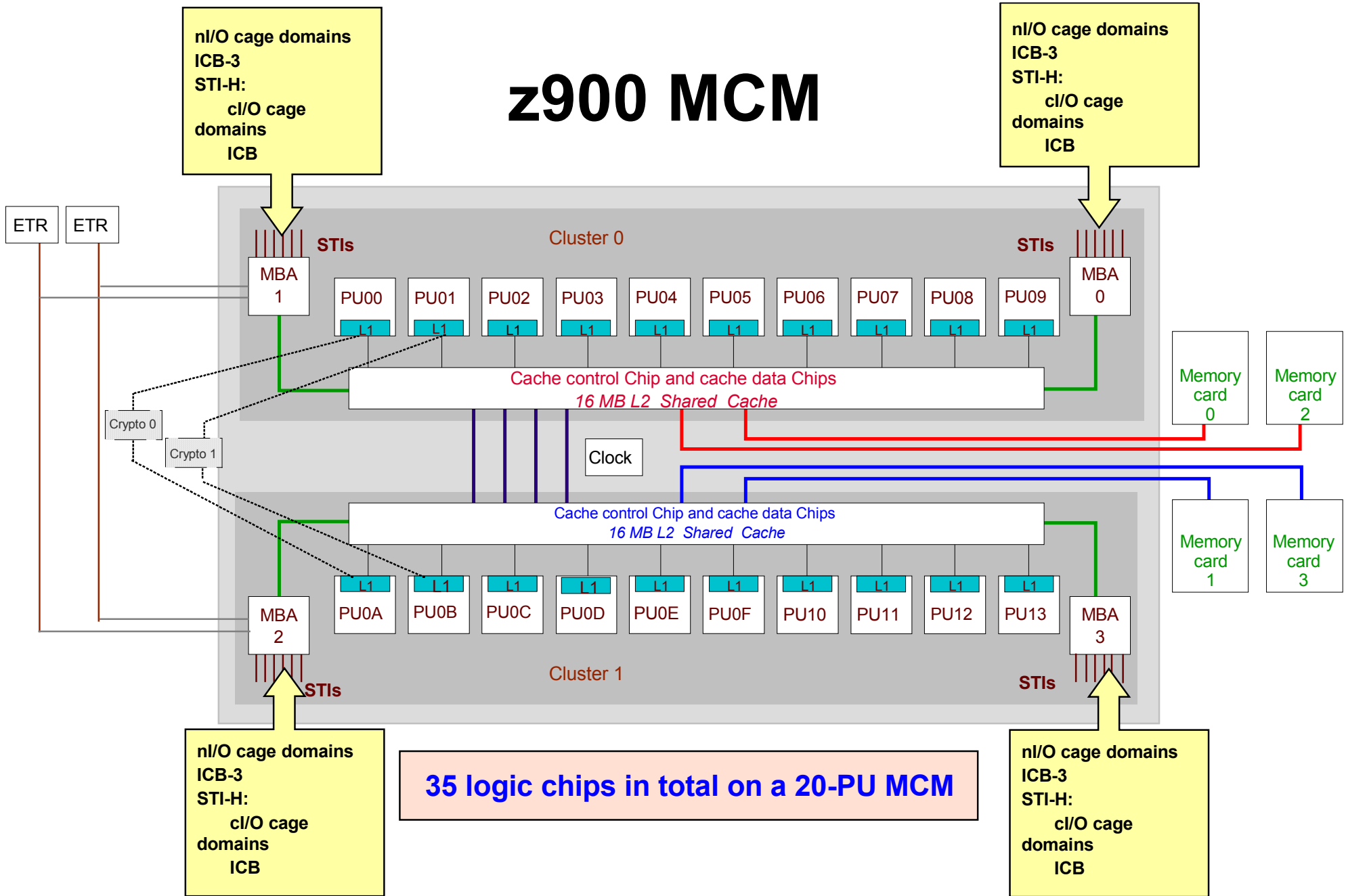
Aufbau eines „Thermal Conduction Module“

WÄRMEABLEITUNG IM TCM



TCM Wärmeübergang

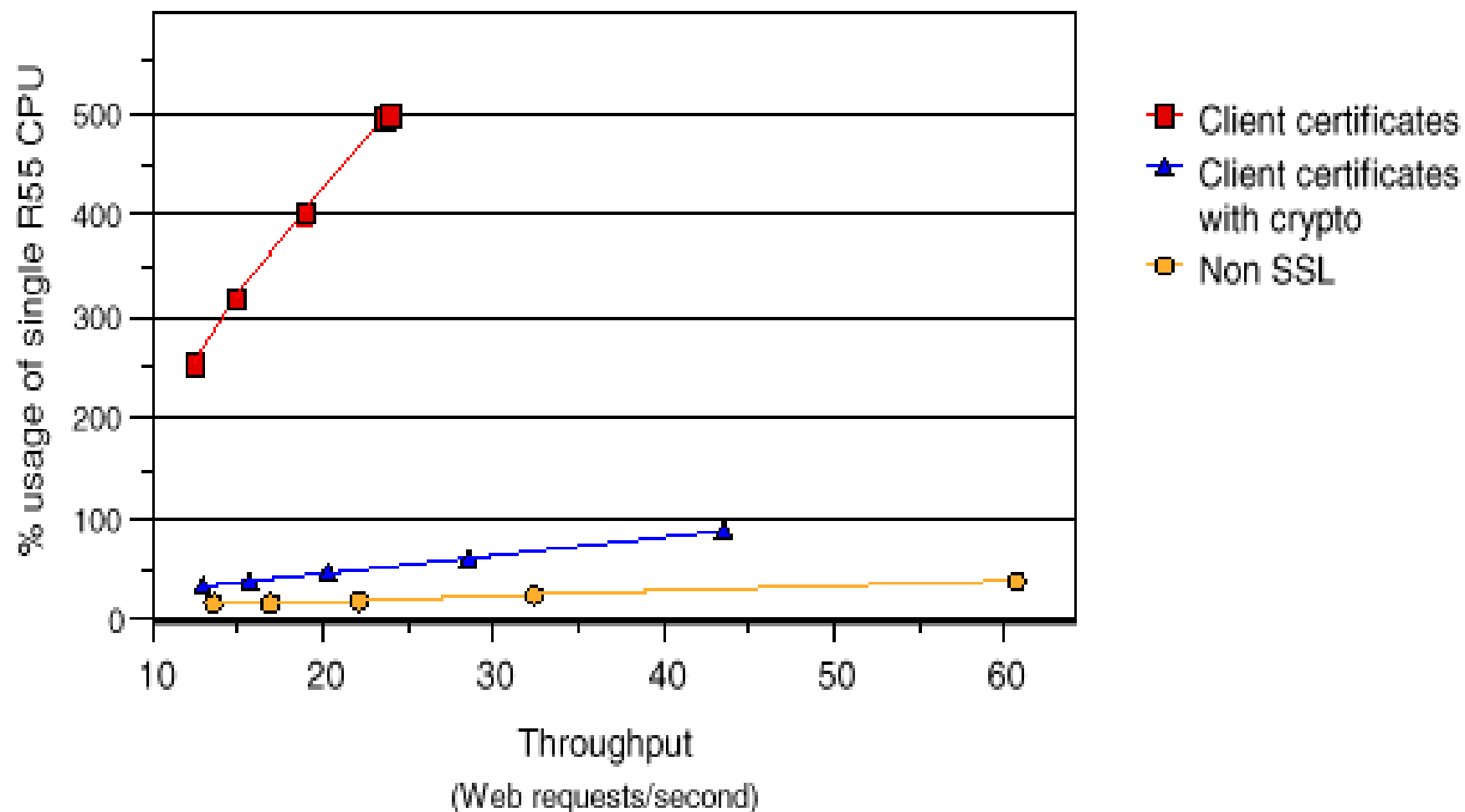
z900 MCM

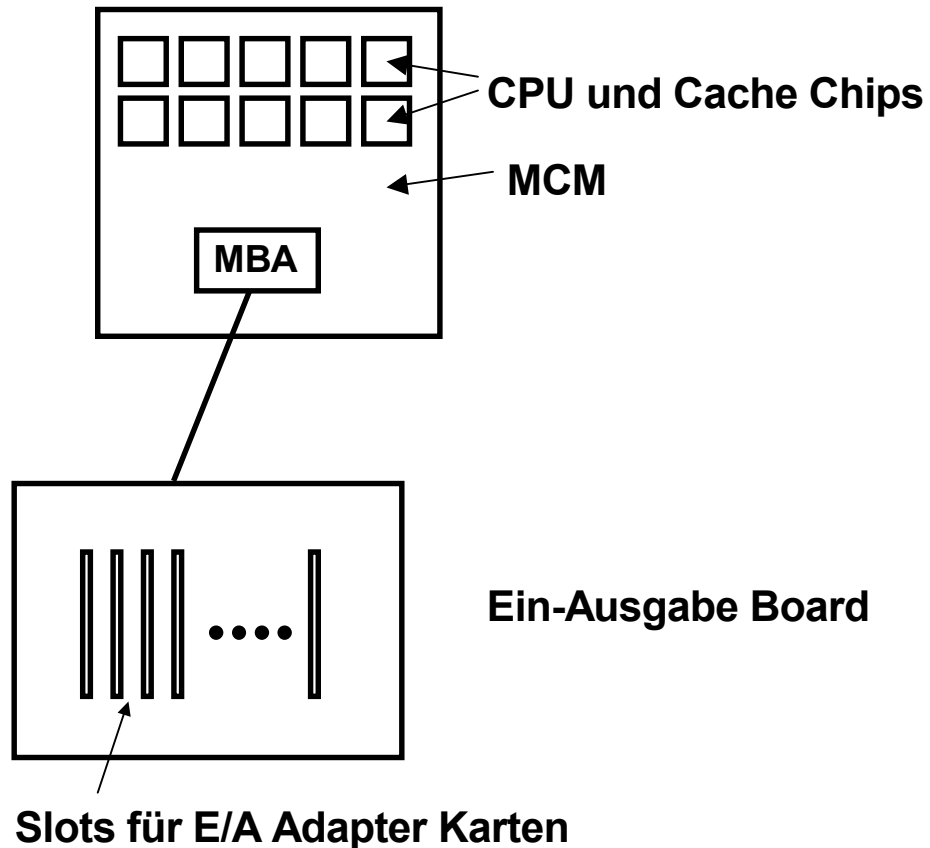


SSL handshakes with client certificates

CWS direct connection

Throughput vs. CPU usage





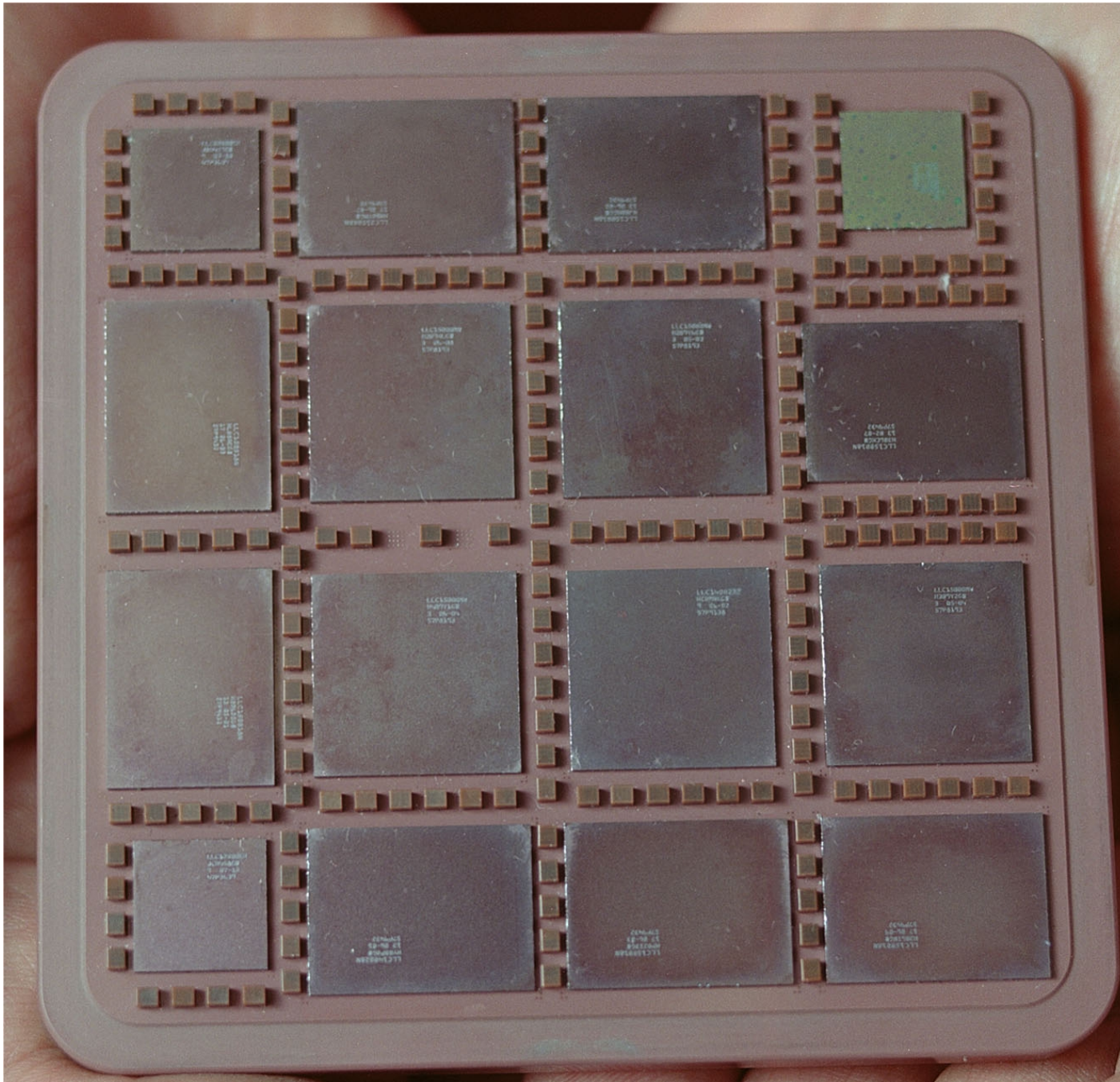
Ein-/Ausgabe Board

Auf dem Multichip Module sitzen neben den CPU- und Cache Chips vier Memory Bus Adapter (MBA) Chips, die eine ähnliche Rolle wie das Southbridge Chip in einem PC übernehmen. Aus jedem MBA werden sechs STI Busse herausgeführt, vergleichbar mit den PCI Bussen in einem PC. Die STI Busse münden in Ein-/Ausgabe Boards, die über STI Slots für die Aufnahme der Ein-/Ausgabeadapter Karten verfügen.

Die wichtigsten E/A Adapter Karten Typen haben Anschlüsse für

ESCON Kanal
 FICON Kanal
 OSA Adapter für Ethernet, ATM,

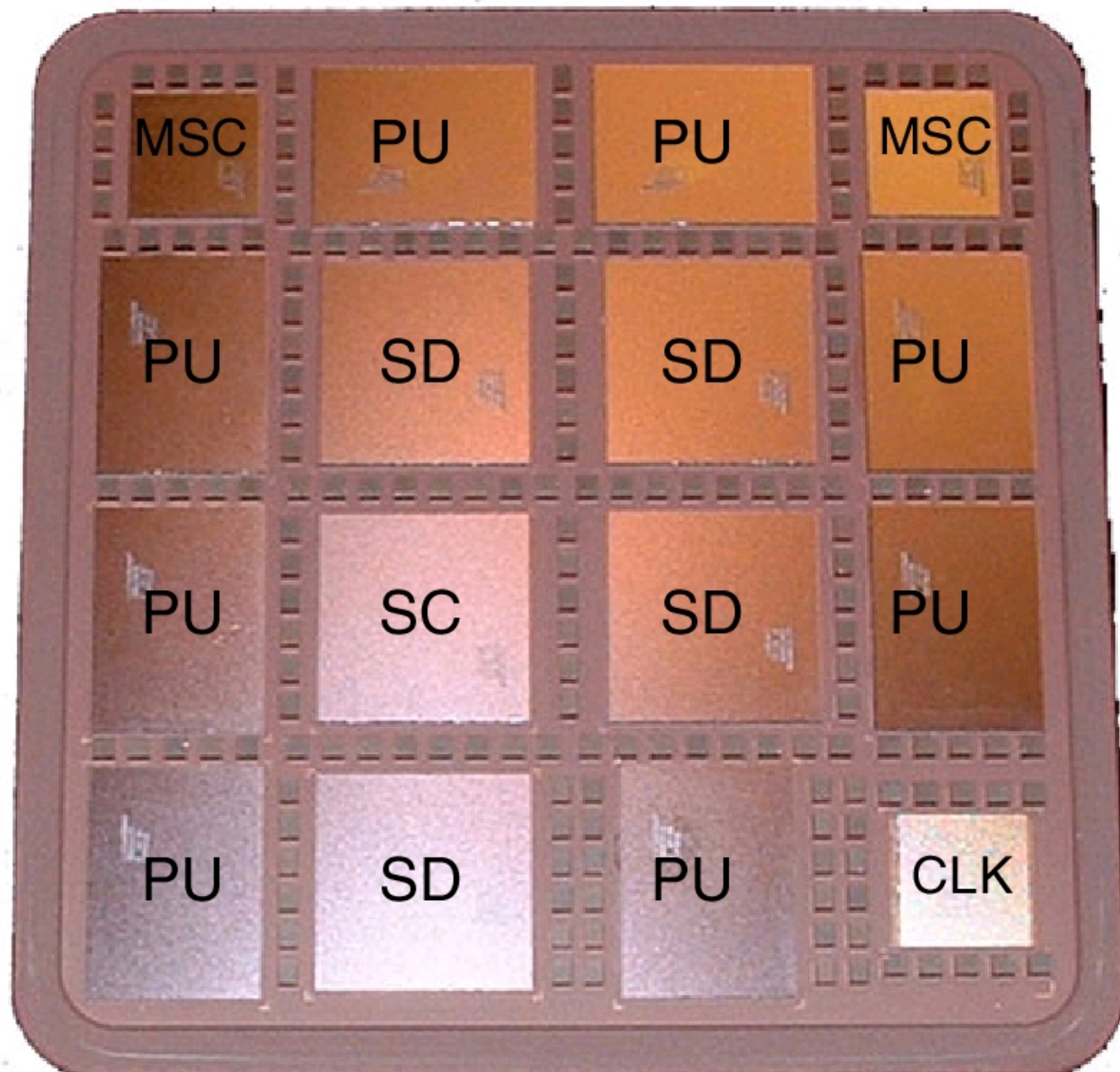


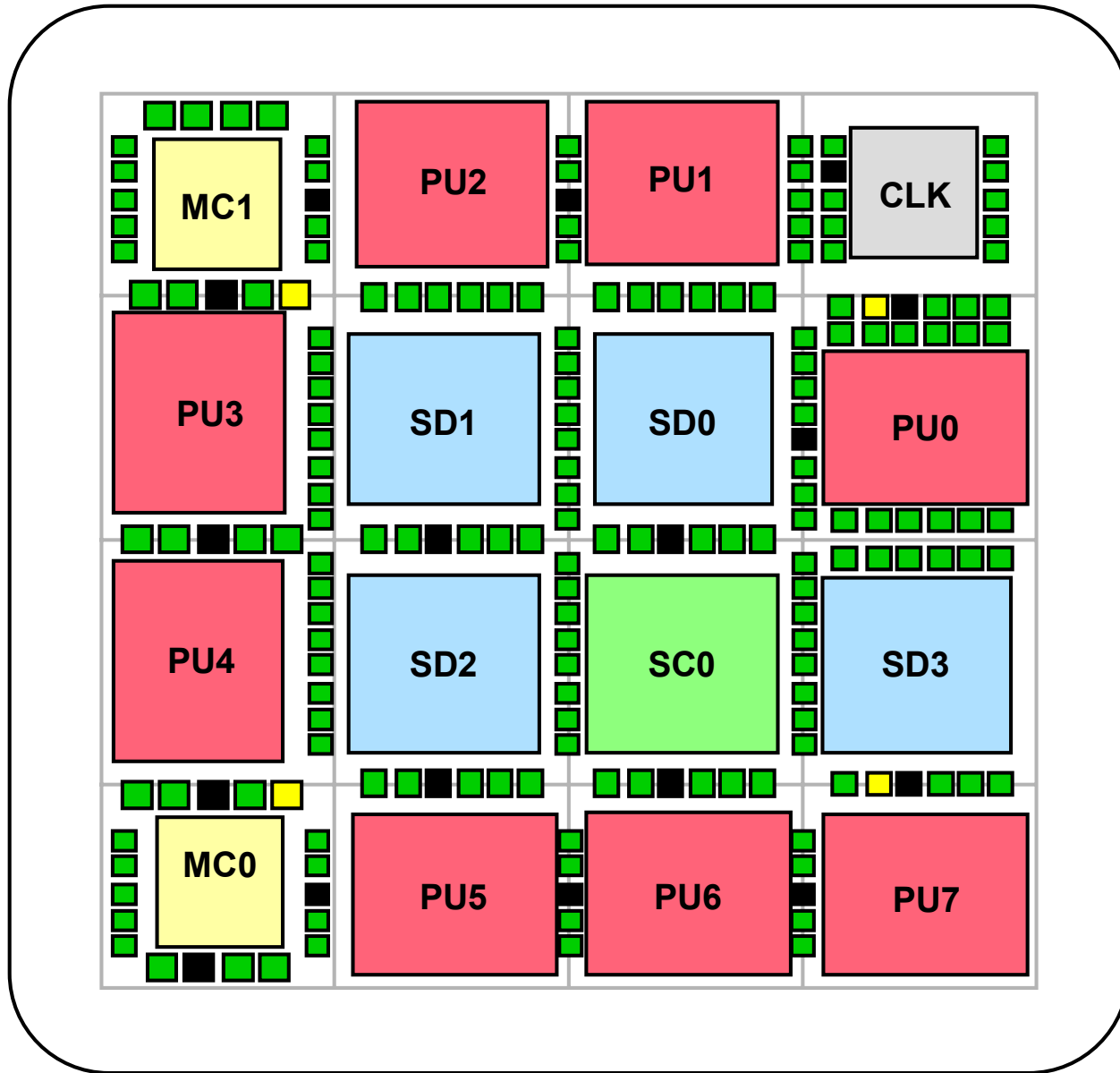


z990 Multichip Module (MCM)

SOI technology

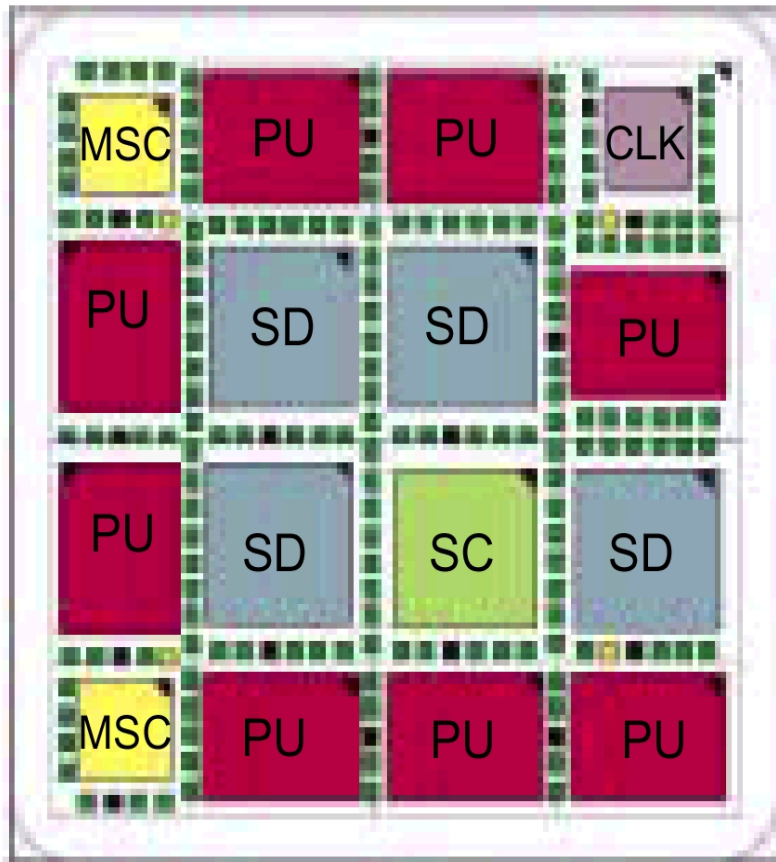
**configuration of one
to four books.
Each book
comprises a MCM
And memory cards
up to 64 GByte per
book**





z990 12 Processor Unit (PU) MCM

- Advanced 93mm x 93mm MCM
 - ▶ 16 chip sites, 185 capacitors
 - ▶ 100 Glass Ceramic layers
 - ▶ 1.3 Volts, 713 Watts
 - ▶ 46% smaller than z900



- CMOS 9SG - SOI chip technology
 - ▶ PU, SC, SD and MSC chips
 - ▶ Copper interconnections, 8 copper layers
- 4 Dual PU, 4 Single PU Chips per MCM
 - ▶ 14.1 mm x 18.9 mm
 - ▶ 122 million transistors/Chip
 - ▶ L1 cache/PU
 - 256 KB I-cache
 - 256 KB D-cache
- 4 System Data (SD) cache chips per MCM
 - ▶ 521 million transistors/chip
 - ▶ 8 MB L2 cache per chip
 - ▶ Single 32 MB L2 cache per MCM
- 1 Storage Control (SC) chip
 - ▶ L2 cache crosspoint switch
 - ▶ L2 access rings to/from other MCMs
 - ▶ L2 access to/from MBAs (off MCM)
- 2 Storage Control (MSC) chips
 - ▶ Memory cards (L3) interface to L2
- 1 Clock (CLK-ETR) chip
 - ▶ CMOS 8SF, 7 copper layers
 - ▶ Clock and ETR Receiver

CMOS 9S-SOI chip Technology
PU, SC, SD and MSC chips
Copper interconnections, 8 copper layers
8 PU chips/MCM
14.1 mm x 18.9 mm
122 million transistors/PU
L1 cache/PU
256 KB I-cache
256 KB D-cache
0.83 ns Cycle Time
4 System Data (SD) cache chips/MCM
17.5 mm x 17.5mm
World's densest chip
L2 cache per Book
521 million transistors/chip
32 MB
One Storage Control (SC) chip
17.3mm x 17.3mm
98 million transistors
Densest I/Os
3692 Power Signal I/Os
L2 cache crosspoint switch
L2 access rings to/from other MCMs
L2 access to/from MBAs (off MCM)
Two Storage Control (MSC) chips
Memory cards (L3) interface to L2
One Clock (CLK) chip - CMOS 8S
Clock and ETR Receiver



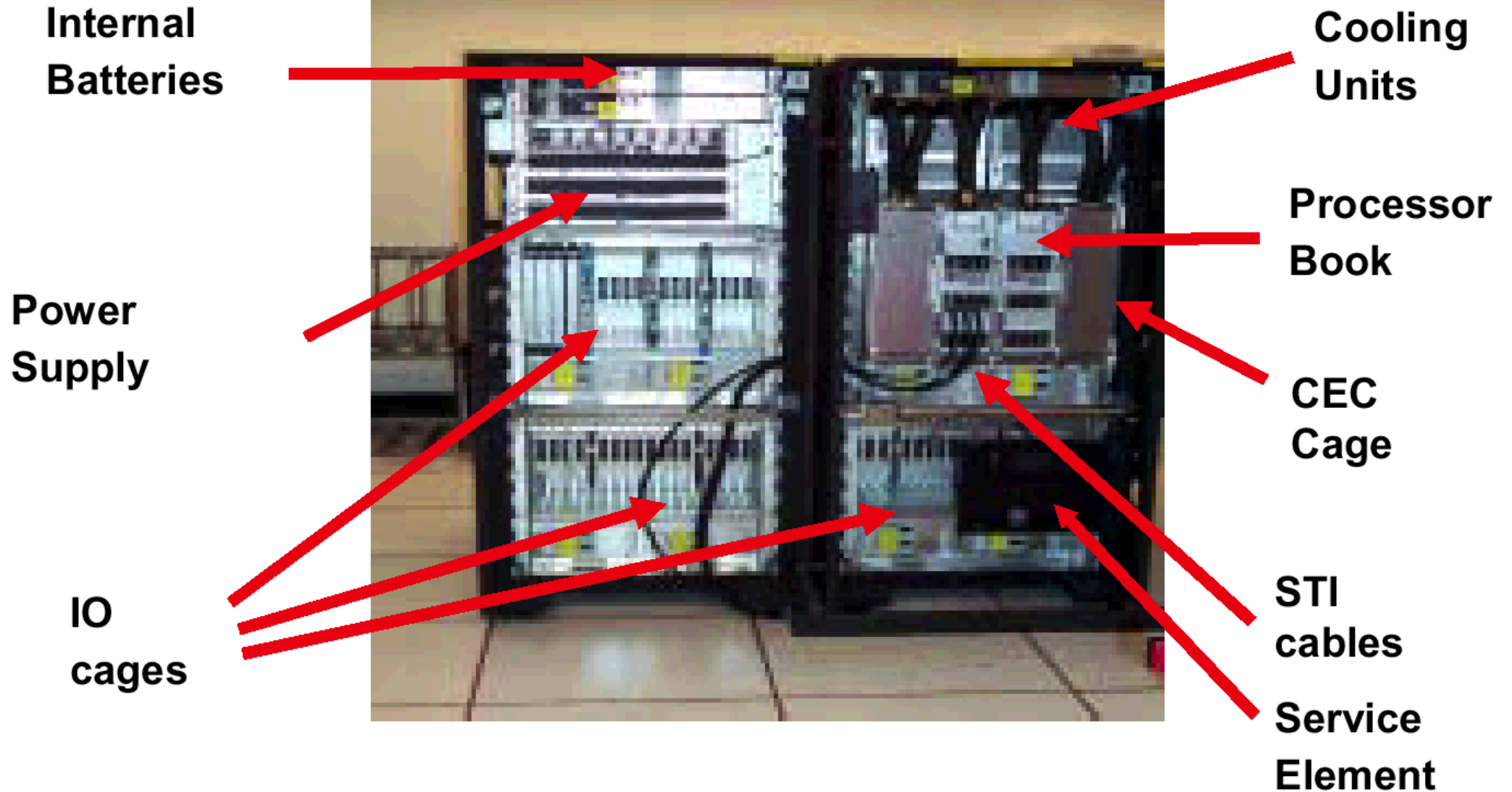
z-Frame

A-Frame



Front View

z990 System



Internal Batteries

Power Supplies

3x I/O cages

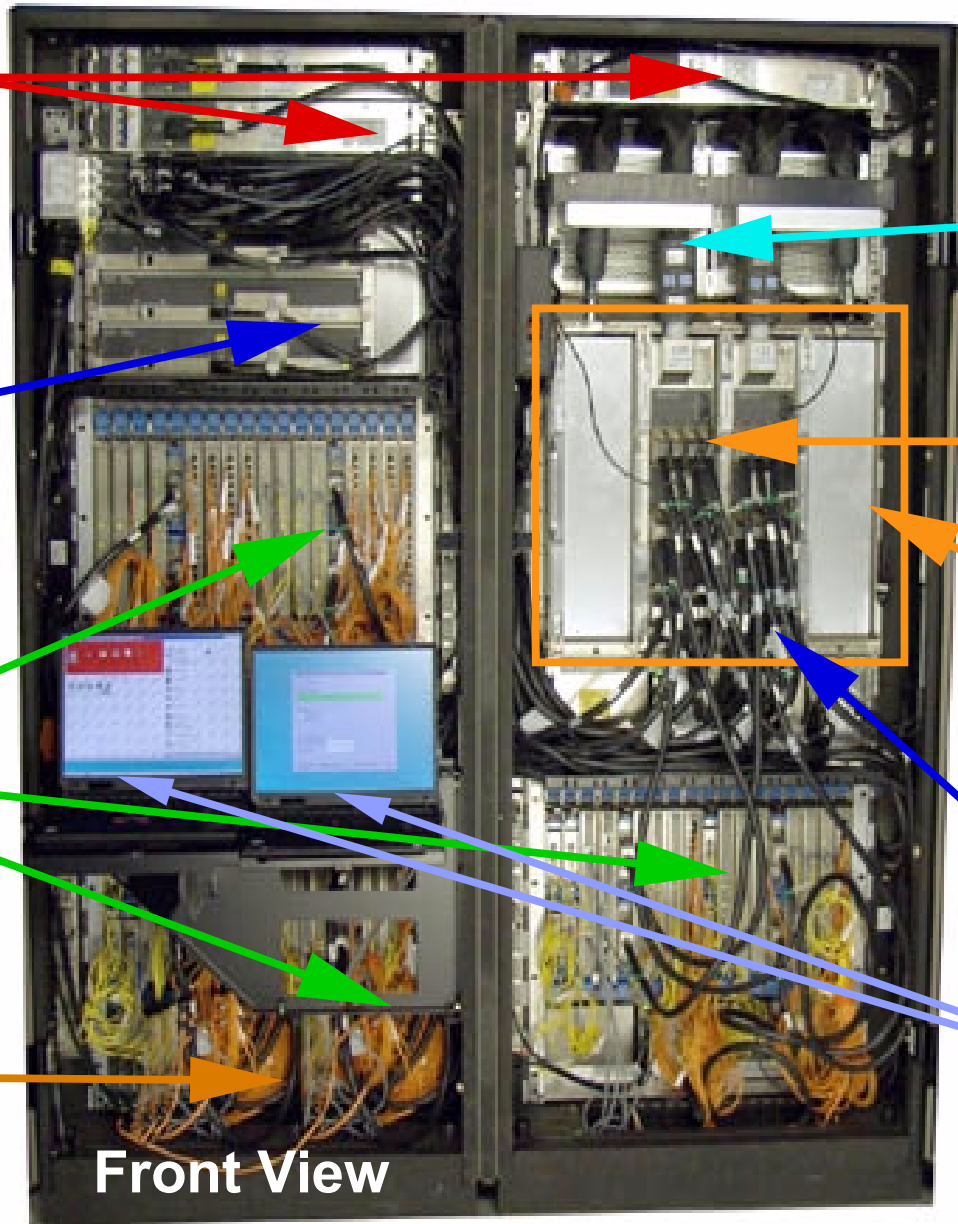
Fibre Quick Connect Feature

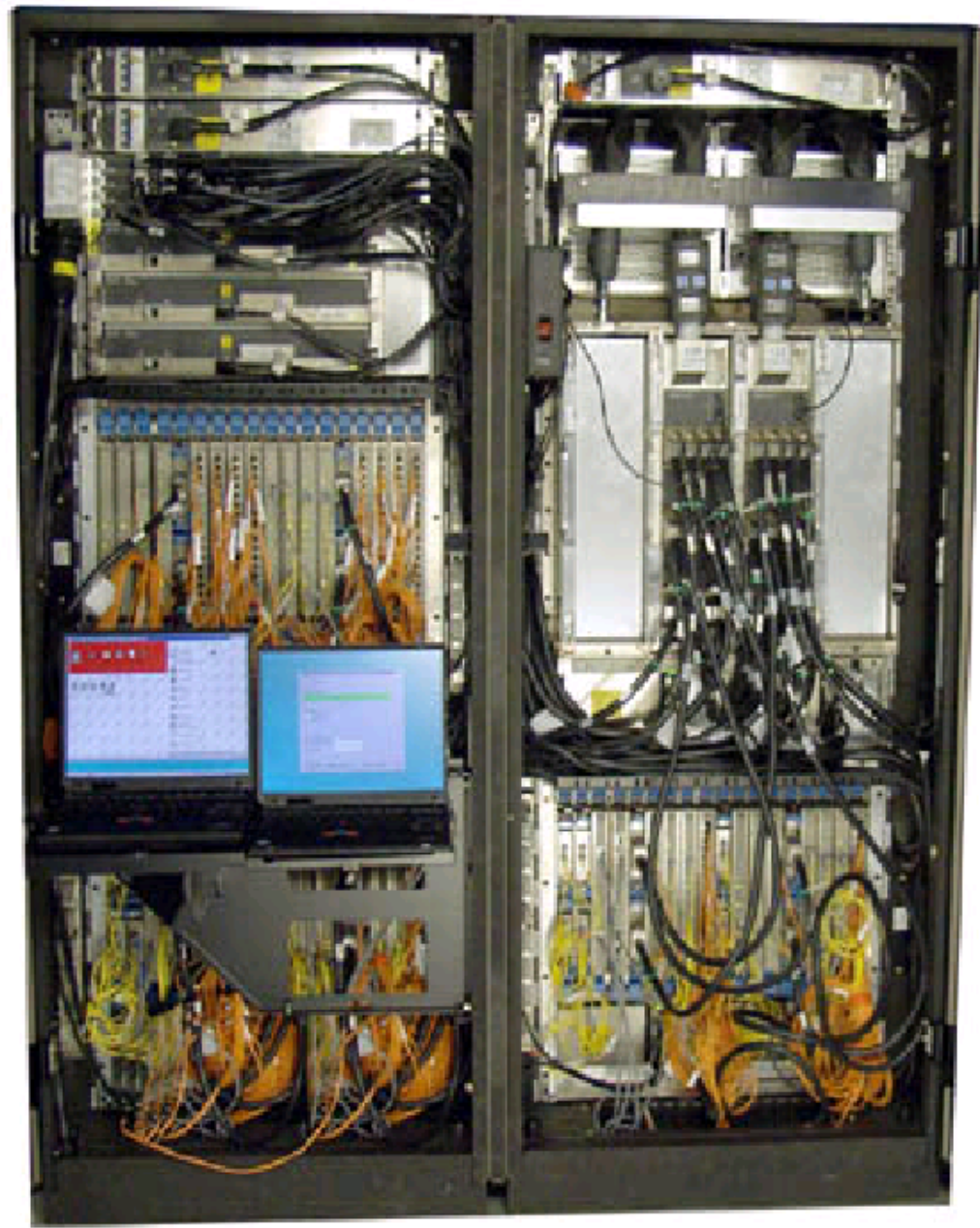
Front View

Hybrid Cooling

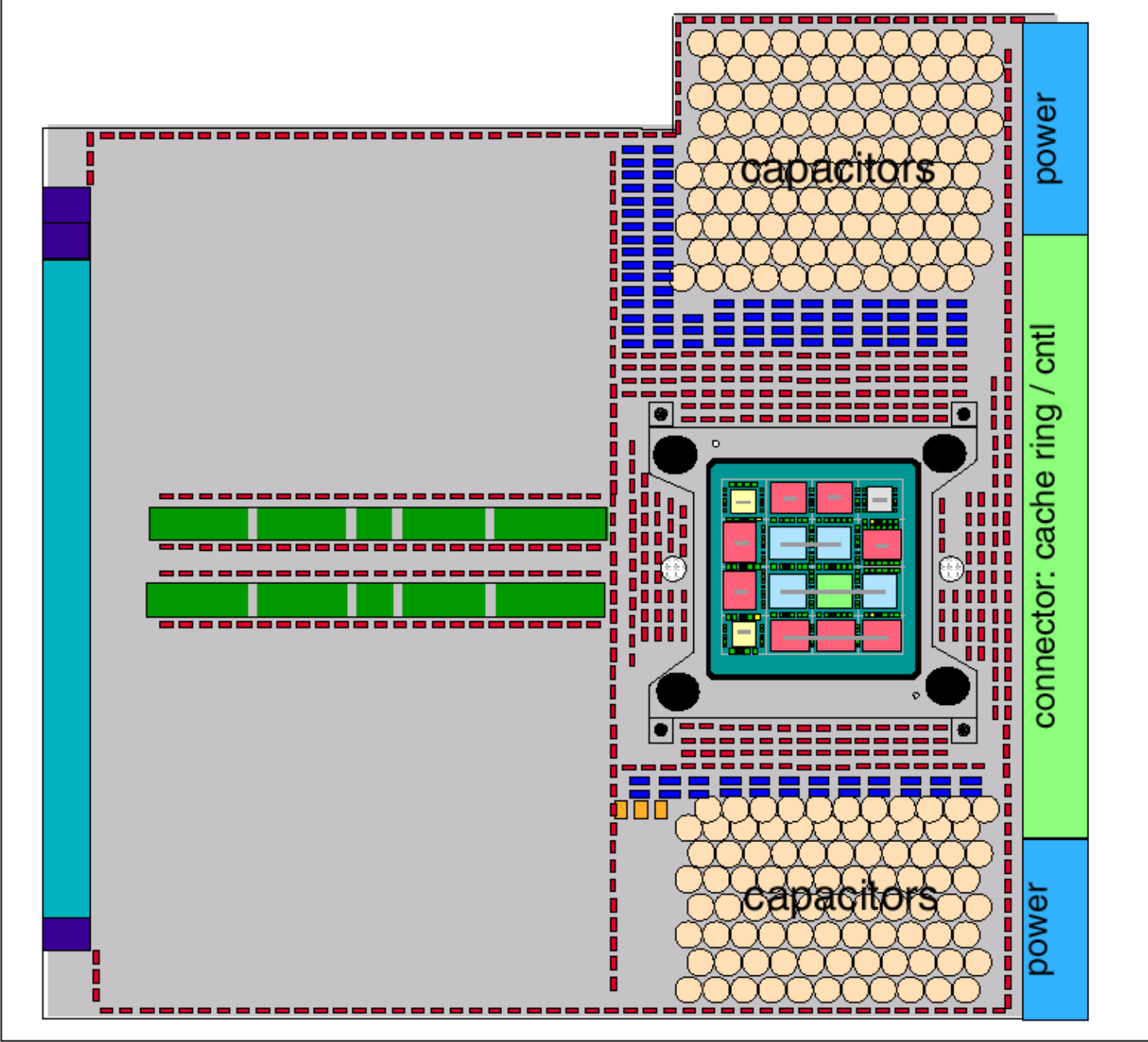
CEC Cage

STI Cable Support Elements





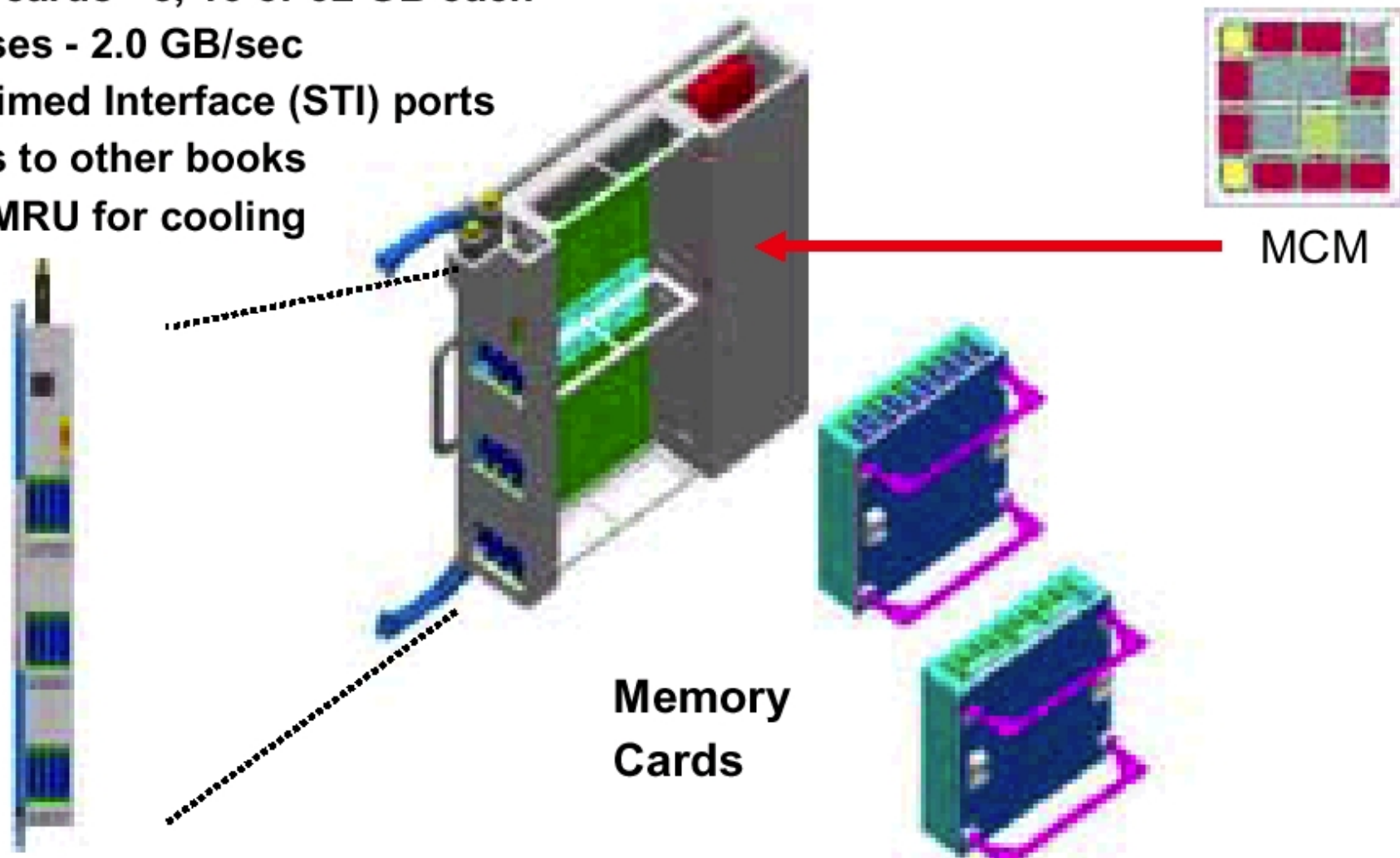




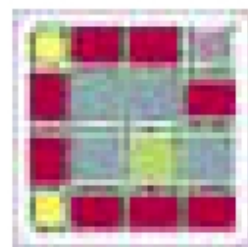
z990 Processor Book

- Multichip module with 12 processor units
- Two memory cards - 8, 16 or 32 GB each
- Channel busses - 2.0 GB/sec
 - ▶ 12 Self-Timed Interface (STI) ports
- Interconnects to other books
- Connects to MRU for cooling

STI
Ports

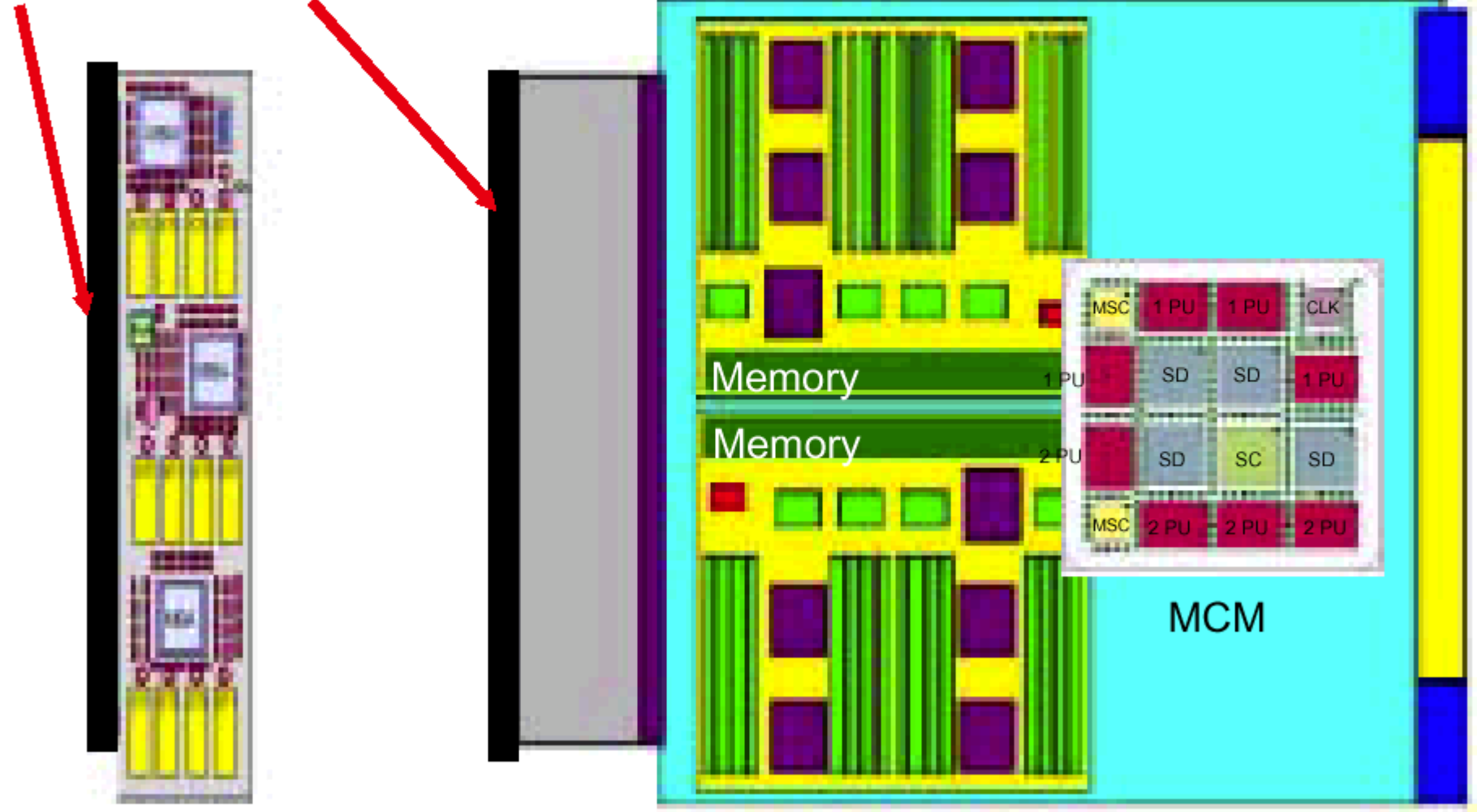


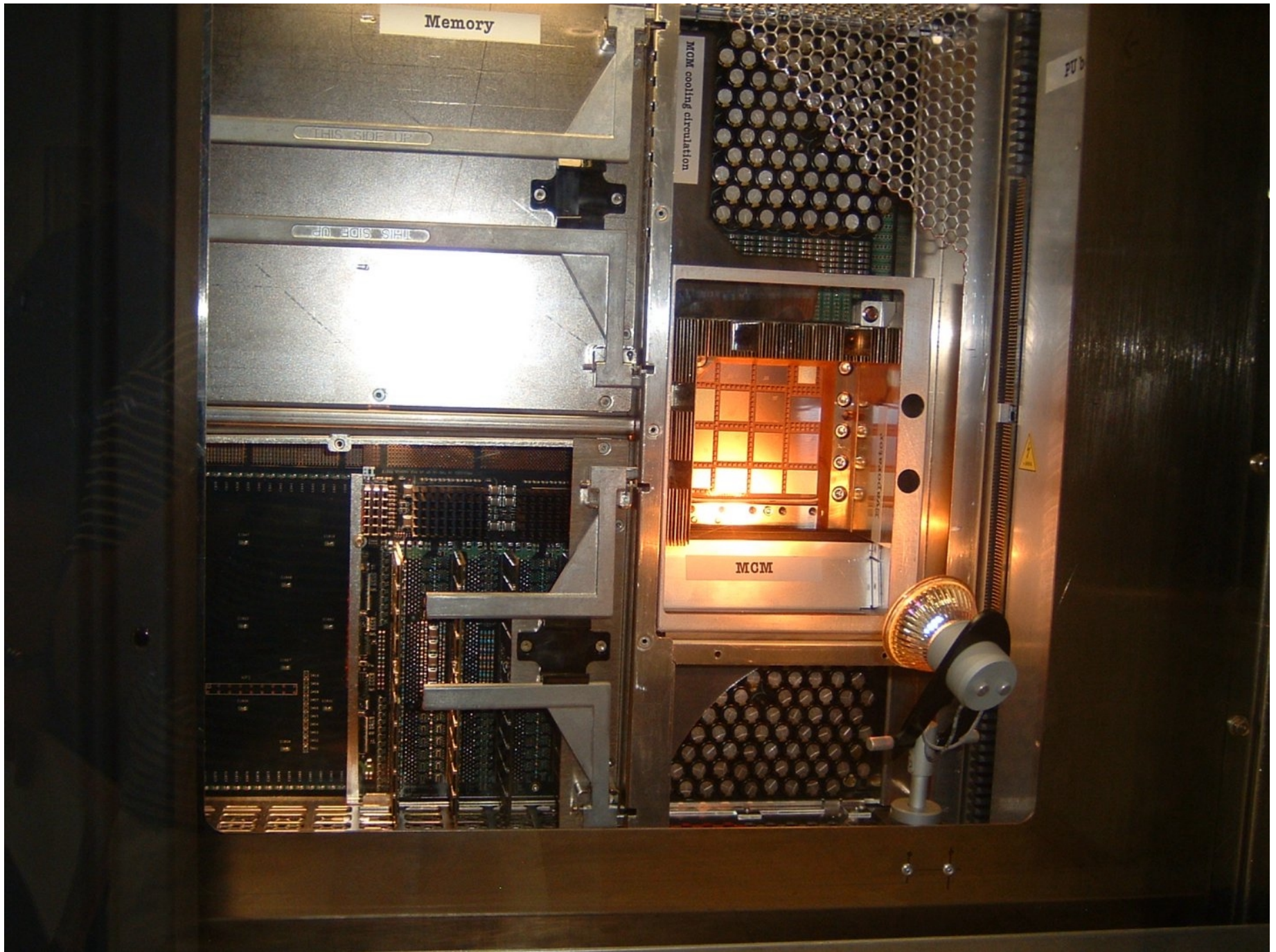
Memory
Cards

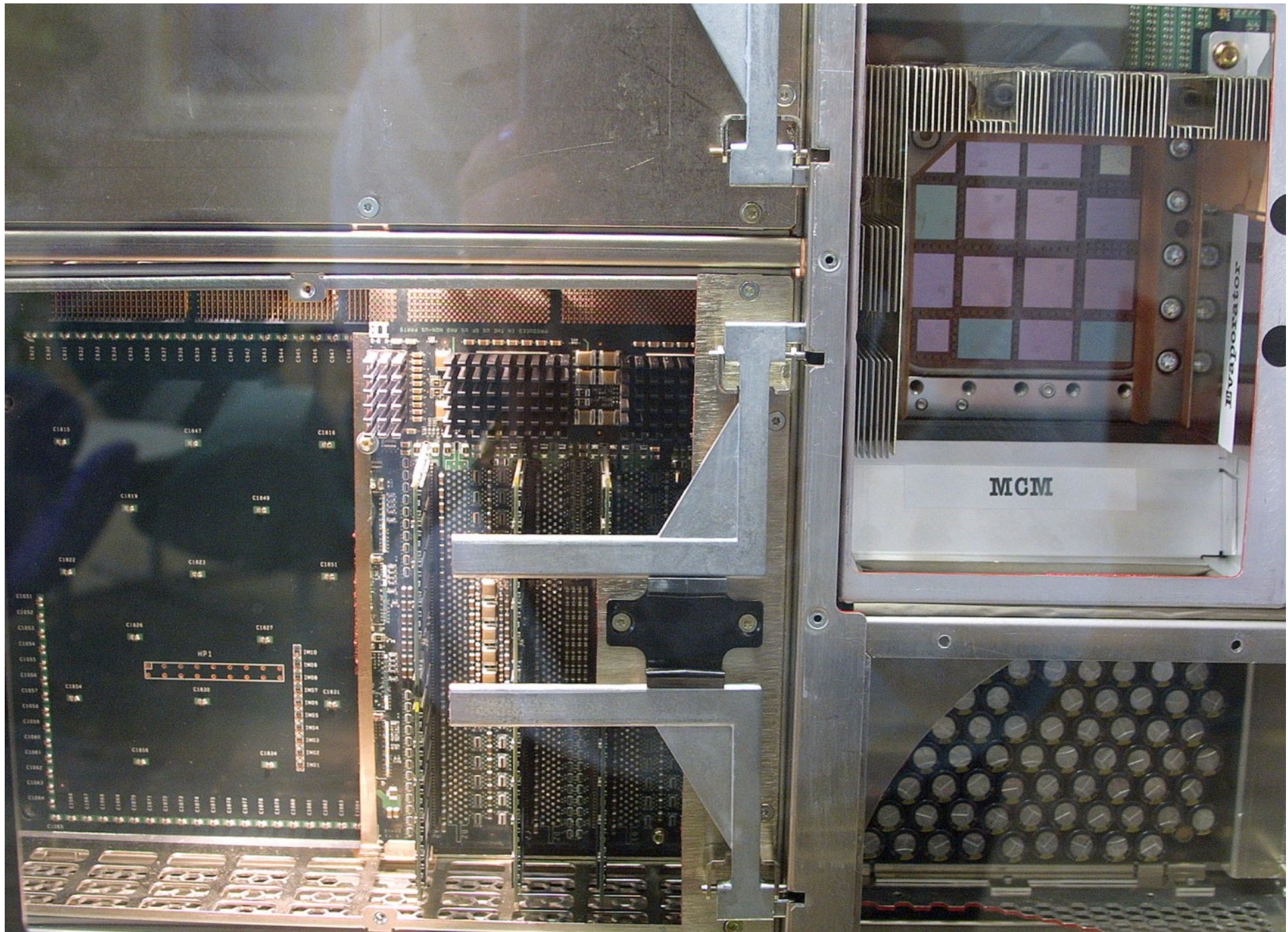


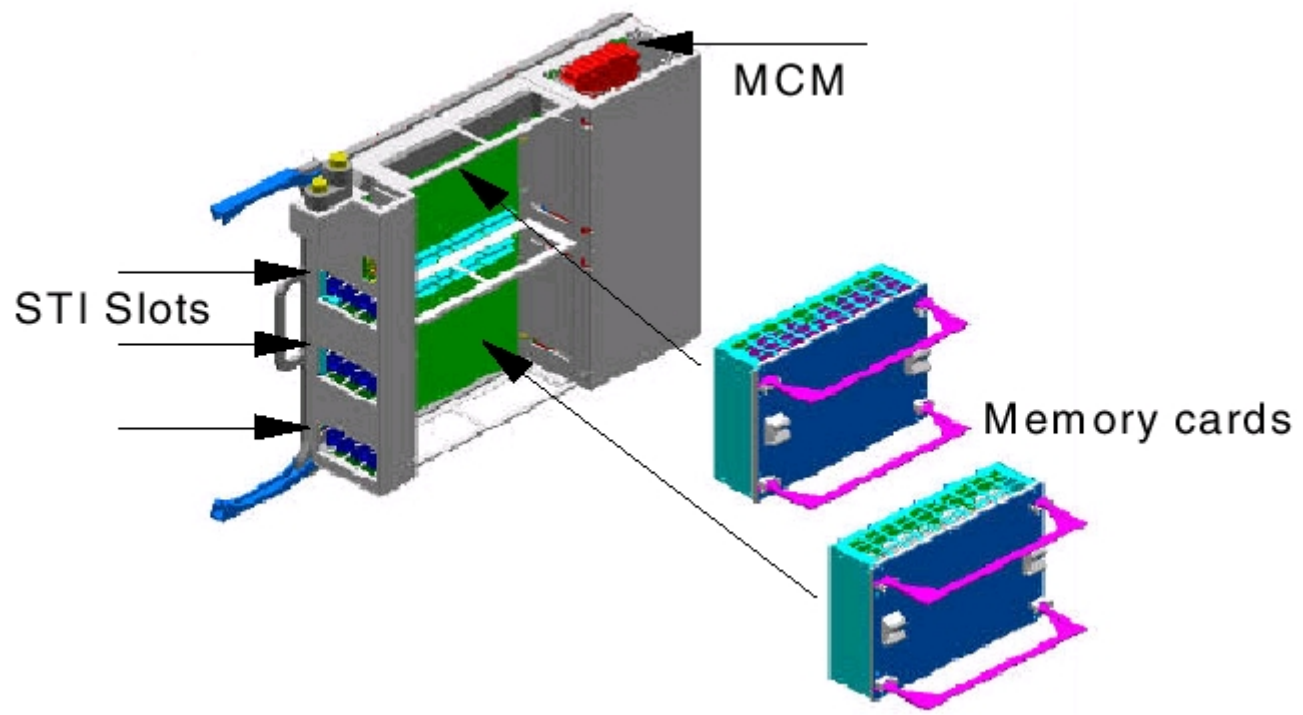
z990 Processor Book Riser Card Memory Bus Adapters (MBAs) and STI Ports

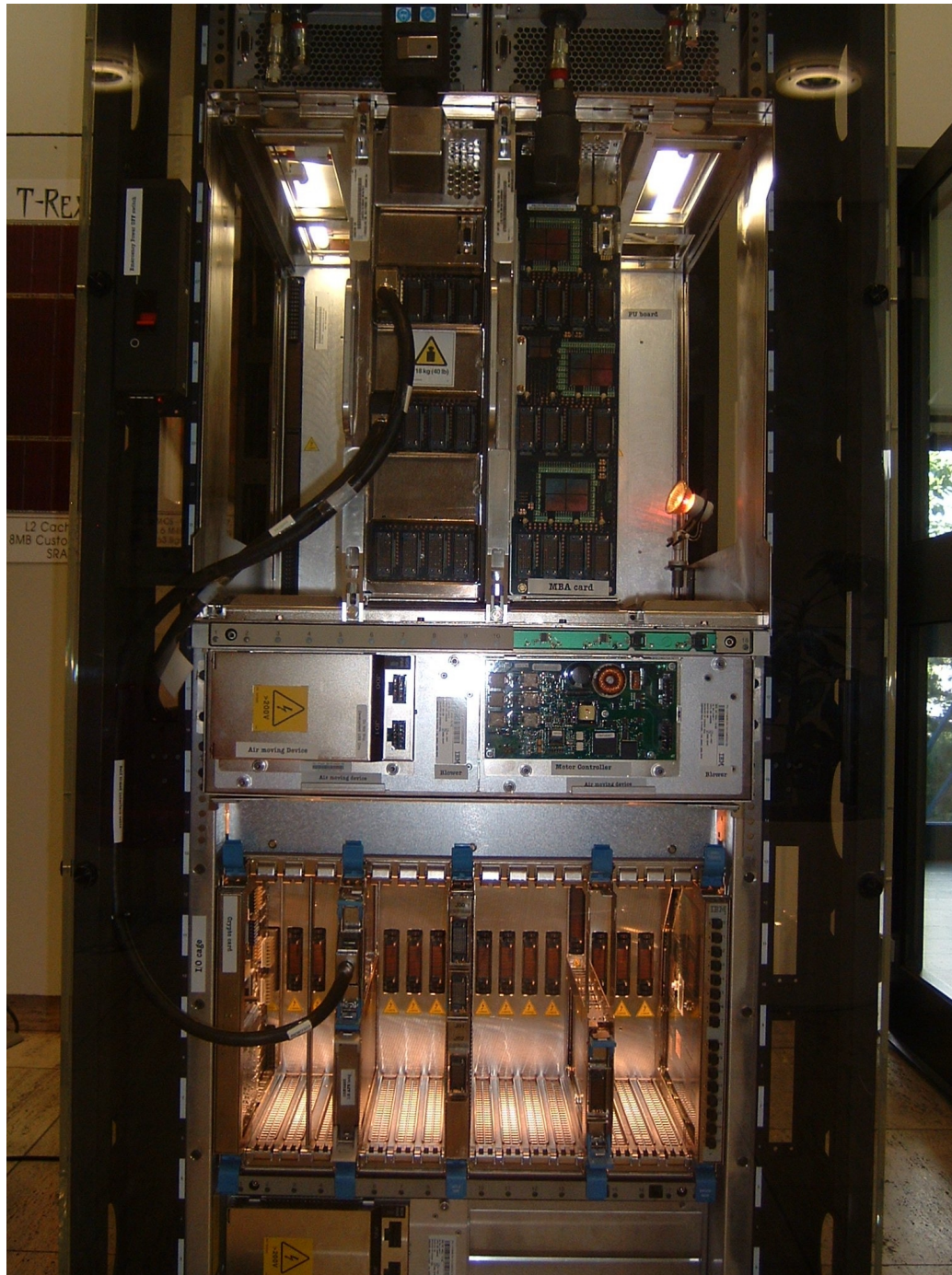
Connector and Slot

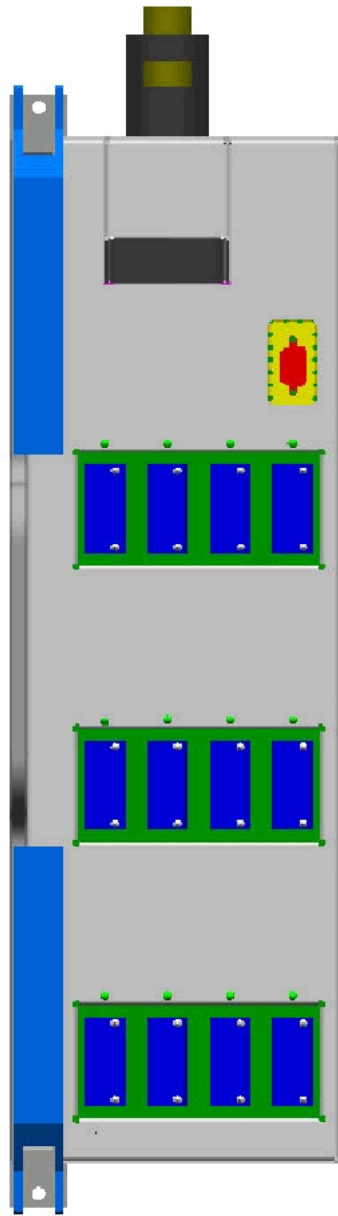








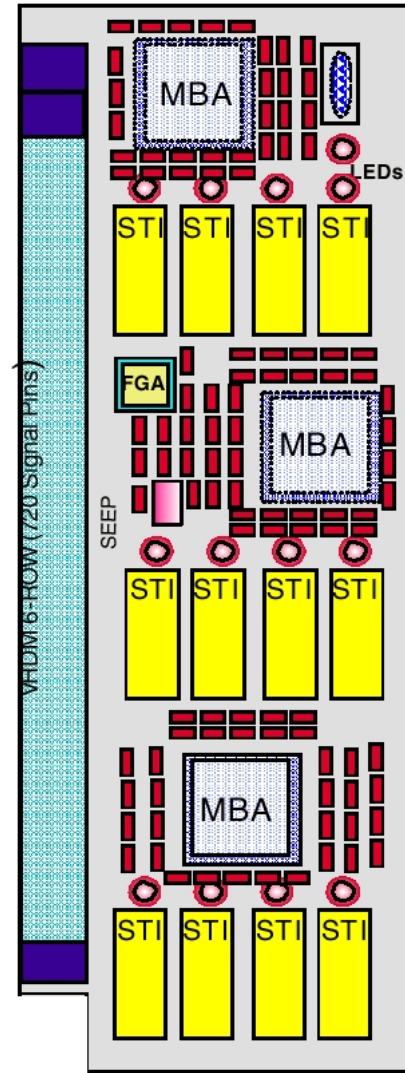
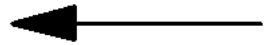




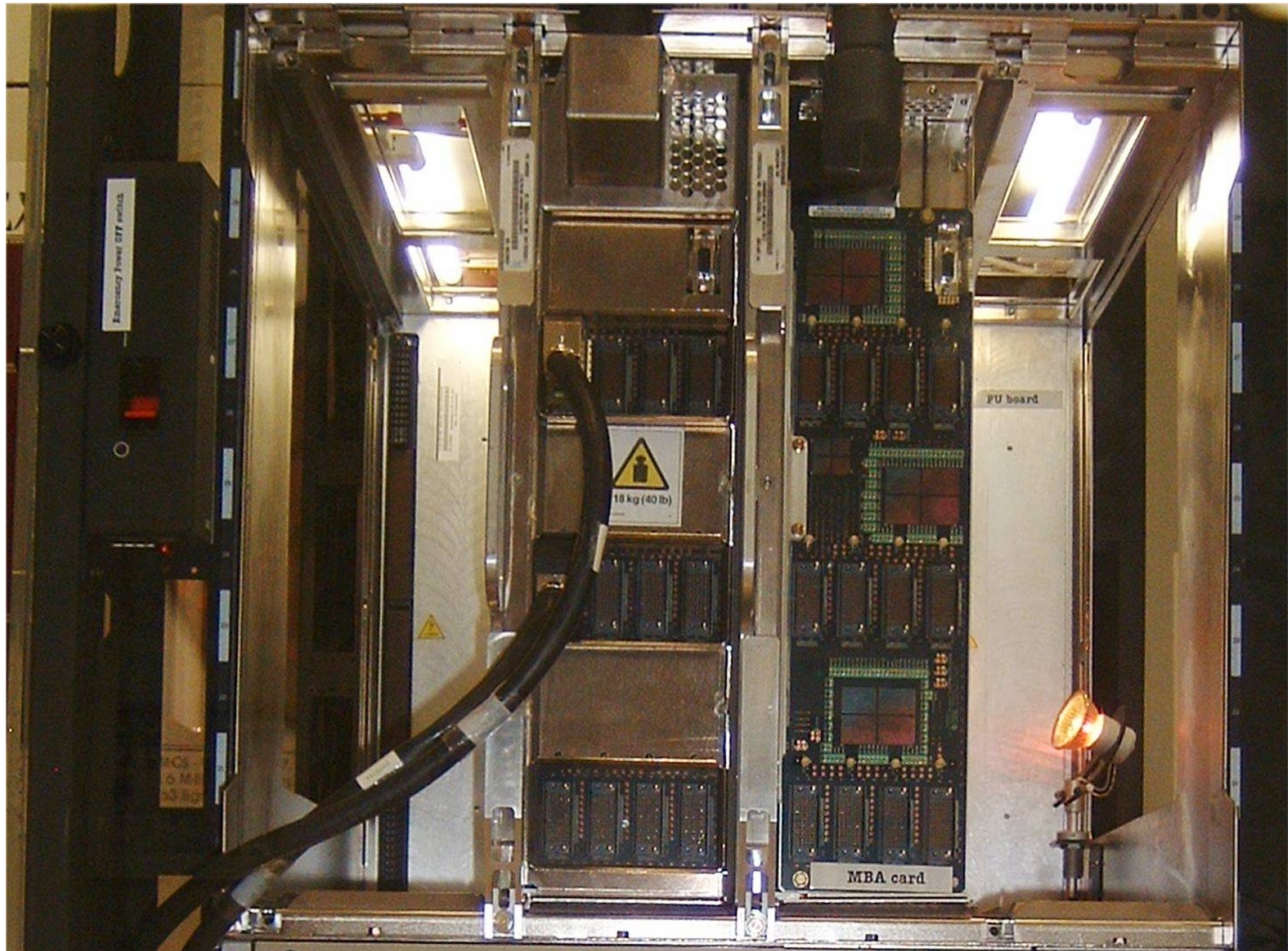
Book front view



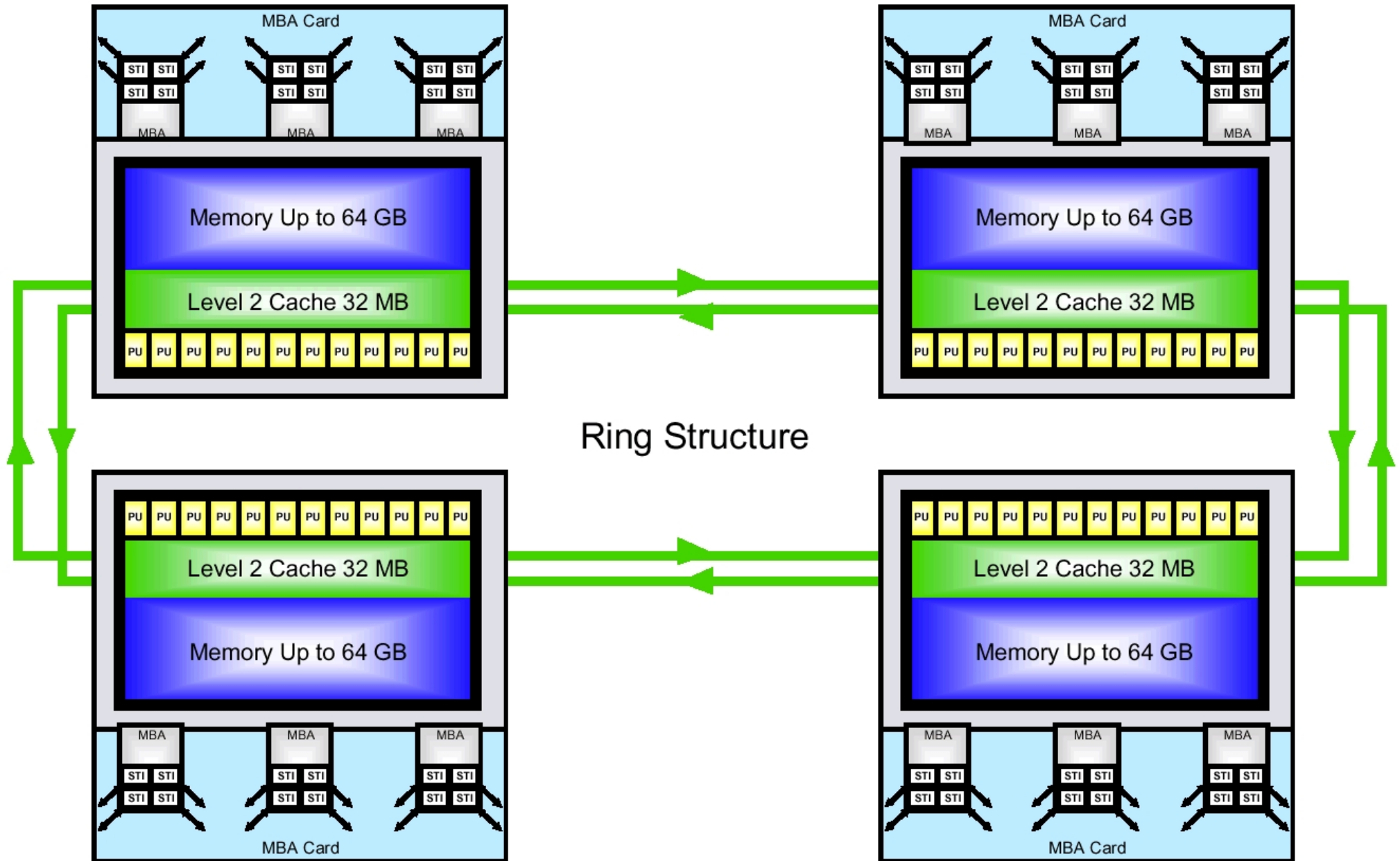
STI connectors

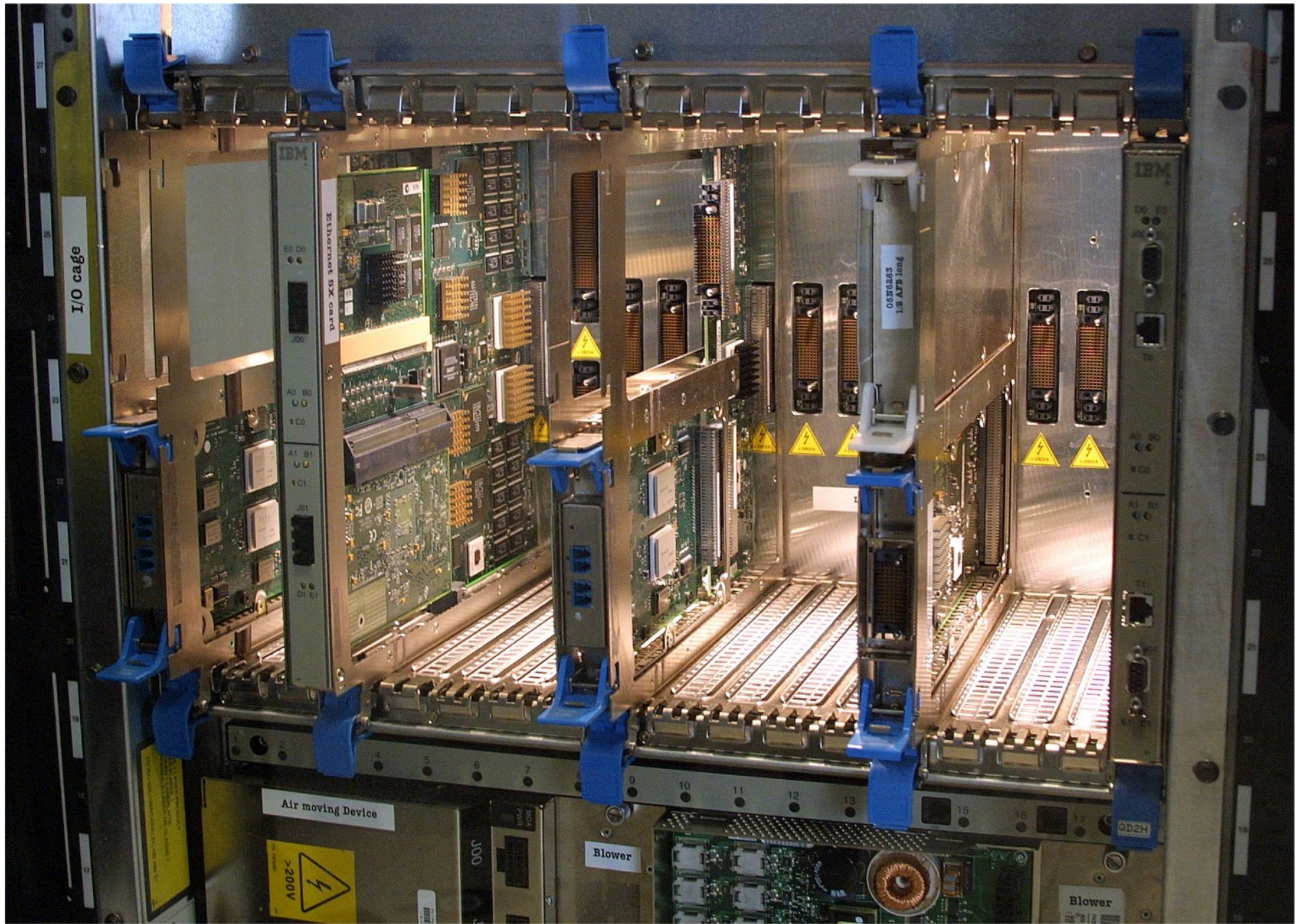


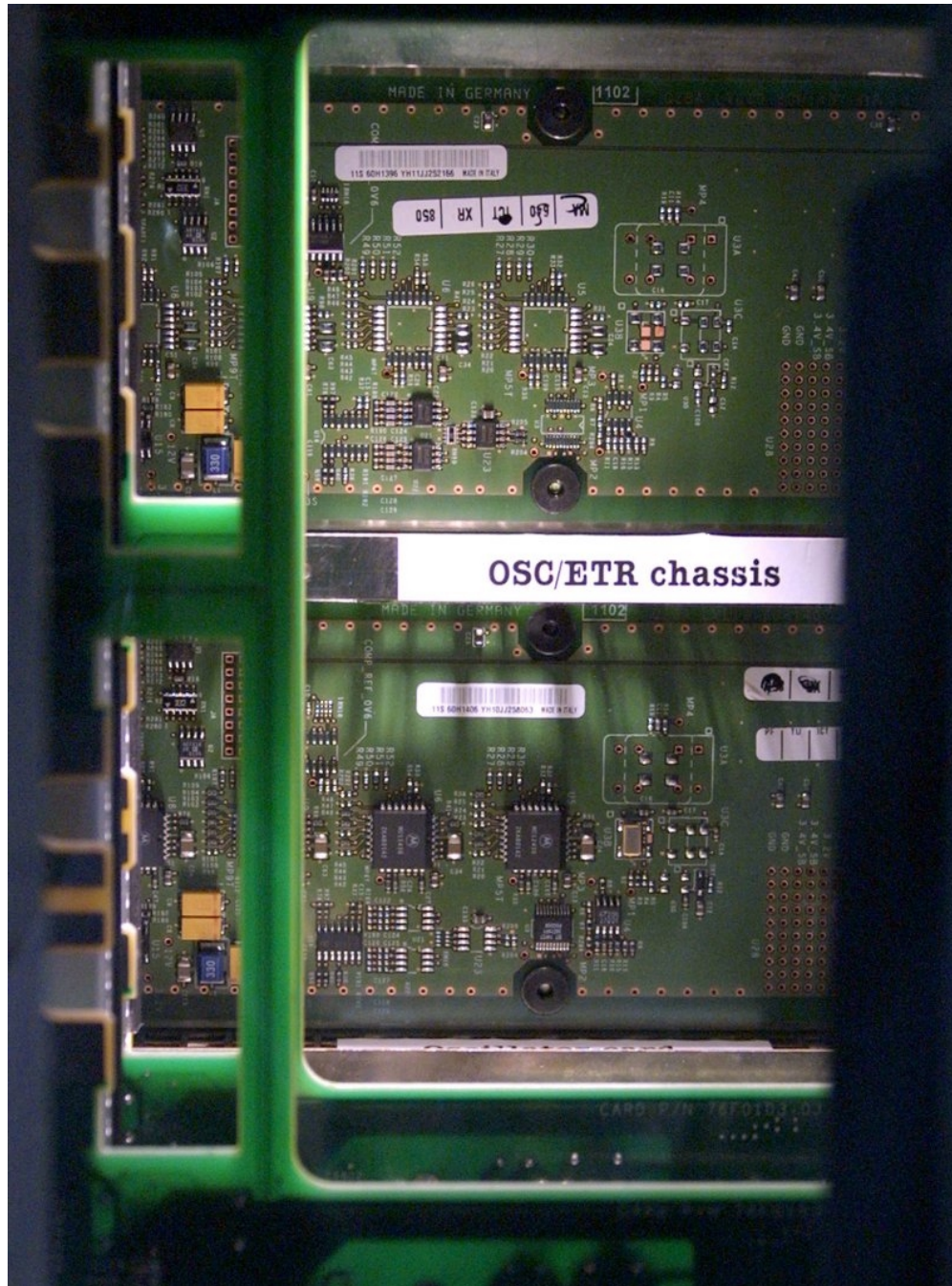
MBA card



z990 Model D32 (GA2)







Hercules

Hercules ist ein open Source Software Paket. Es emuliert die System/390 und zSeries Architektur.

Hercules läuft auf einem regulären, leistungsfähigen PC unter Linux, Windows 98, Windows NT und Windows 2000.

Einzelheiten:

<http://www.conmicro.cx/hercules/>

<http://neuro2.med.uni-magdeburg.de/~markgraf/mvs/doc/hercfaq.html>